everyday genius

MT7622B Datasheet

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Overview

MT7622B is a highly integrated wireless network router system-on-chip used for high wireless performance, home entertainment, home automation and so on.

Applications:
- Internet service router
- Wireless router
- Home security gateway
- Home automation
- NAS devices
- Wireless audio

MT7622 is fabricated with advanced silicon process and integrates a Dual-core ARM® Cortex-A53 MPCoreTM operating up to 1.35GHz and more DRAM bandwidth. This SoC also includes a variety of peripherals, including SGMII, RGMII, PCIe2.0, USB2.0(Host) ,USB3.0(Host) ports, and 5-port 10/100 switch. To support popular network applications, MT7622B also implements 2.5Gbps HSGMII and 1Gbps RGMII Ethernet interface, embedded a 5-ports 10/100 switch and 802.11n 2.4GHz 4T4R WLAN radio, 802.11ac WLAN connection can be supported thru its PCIe port.

Besides the connectivity features, the hardware-based NAT engine with QoS embedded in MT7622B transporting the audio/video streams in higher priority than other non-timely services also enriches the home entertainment application. The SFQ separating P2P sessions from audio/video ones so that MT7622B guarantees the streaming service.

With the advanced technology and abundant features, MT7622B is well positioned to be the core of next-generation Smart WiFi AP router, and home gateway systems.

Key Features

- Embedded Dual-core ARM® Cortex-A53 MPCoreTM operating at 1.35GHz
  - 32KB L1 I-Cache and 32KB L1 D-Cache
  - 512KB unified L2 Cache
  - NEON/FPU
  - DVFS technology
- 16-bit data width for DDR2(x16) and DDR3(x8, x16)
- NOR(SPI), NAND Flash(SLC, SPI), MSDC(4-bits), eMMC4.4.1
- USB3.0 Host x 1
- USB2.0 Host x 1
- PCIe2.0 Host 1-lane x 2
- SATA3.0 x 1
- SPI, I2C, UART Lite, JTAG, MDC, MDIO, GPIO, PWM
- Samba R/W more than 100MB/s through SATA
- One HSGMII(1/2.5Gbps)/RGMII/MII interface
- WiFi
  - Lead in 4x4 11n FEM integration
  - Airtime Fairness
  - Spectrum Analyzer
- Fast Ethernet Switch
  - 5 ports with full-line rate
  - 5-port 10/100Mbps MDI transceivers
- HW storage accelerator
  - HW NAT (Etheren/WiFi)
  - Wired speed
  - IPv4 routing, NAT, NAPT
  - IPv6 routing, DS-Lite, 6RD, 6to4
- HW QoS
  - 64 hardware queues to guarantee the min/max bandwidth of each flow.
  - Seamlessly co-work with HW NAT engine.
  - SFQ w/ 1k queues.
- Security
  - Secure boot
  - Crypto Suite
  - Anti Clone
- Green
  - Intelligent Clock Scaling (exclusive)

DDR: ODT off, Self-refresh mode

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Functional Block Diagram

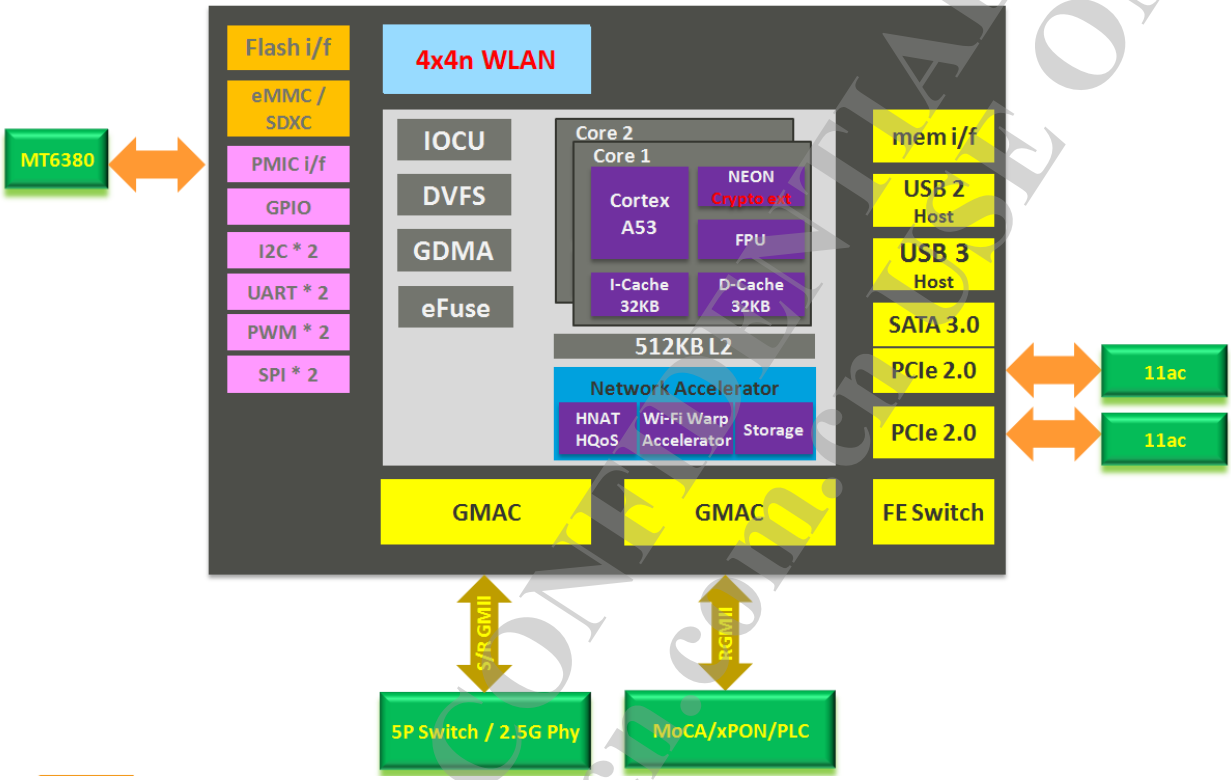

Figure 1-1 Chip Block Diagram

Figure 1-2 4x4n WLAN Block Diagram

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Document Revision History

Revision	Date	Author	Description
Preliminary	2016-11-01	Leon Chung	Initial Release
1.0	2017-10-27	PeterCT Wu	Fix DDR size and VCCK voltage Formal release to DMS
1.1	2017-12-19	PeterCT Wu	Update WIFI statement Add pin description
1.2	2018-3-19	PeterCT Wu	1. Update pin default 2. Add 4x WLAN block diagram 3. Add operation condition
1.3	2019-6-27	PeterCT Wu	1. Fix pin typo on USB and UART 2. Remove I2C@1.8V
1.4	2020-02-20	PeterCT Wu	Add GPIO drive/sink capability on MDI_*
1.5	2020-06-05	PeterCT Wu	1. Add MDIO AC Electrical Characteristic 2. Modify Power-on Sequence
1.6	2020-07-03	PeterCT Wu	1. Update Pin Description
1.61	2020-10-06	PeterCT Wu	Update Pin Location
1.7	2020-12-11	PeterCT Wu	Add DC electrical characteristics

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1 General Features

1.1 Platform Features

- **AP MCU subsystem**
  - Dual-core ARM® Cortex-A53 MPCoreTM operating at 1.35 GHz
  - NEON processing engine with Advanced SIMD and Floating-point Extension
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 0.95V to 1.35V
  - Cryptography Extension
  - IO Coherence
- **WBSYS MCU subsystem**
  - Andes N9 processor with 32KB I-cache, 16KB D-cache
- **External memory interface**
  - Supports DDR2, DDR3
  - Supports 16-bit data bus width
  - Memory clock up to 533MHz(DDR2) and 800MHz(DDR3)
  - Supports self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Supports dual rank memory device
  - Advanced bandwidth arbitration control
  - 2 PCIe2.0 (2rd port is shared w/ SATA3.0)
  - 1 SATA3.0 (eSATA Gen2)
  - 2 PCIe2.0 1 USB3.0 w/. 64 endpoints
  - 1 USB2.0 high-speed host mode supporting 2 Tx and 2 Rx endpoints
  - UART for external devices and debugging interfaces
  - SPI master for external devices
  - I2C to control peripheral devices,
  - General Purpose Input/Output
  - 2 sets of memory card controller supporting(SD/ SDHC/ MS/ MSPRO/ MMC and SDIO2.0/3.0 protocols)
- **Operating conditions**
  - Core voltage: 1.15V
  - Processor DVFS voltage : VPROC 0.95V~1.35V (Typ. 1.15V; Sleep mode 0.9V) ; VPROC_SRAM voltage : 1.15 ~ 1.35V
  - I/O voltage: 1.8V/3.3V
  - DRAM Memory: 1.35V/1.5V/1.8V
  - eMMC NAND and SLC-NAND: 1.8V
  - Clock source: 25MHz, 32.768kHz(option)
- **Package**
  - FCCSP 15x15mm 426 balls
  - Ball pitch: 0.65mm

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1.2 Wireless Connectivity Features

- **4x4n WiFi**
  - IEEE 802.11 b/g/n compliant
  - Support 5MHz, 10 MHz, 20MHz, 40MHz bandwidth in 2.4GHz band
  - Throughput (cut-through architecture)
    - HT40 : TCP T-Put 397.2 Mbps (Efficiency 66.20%)
    - VHT40 : TCP T-Put 560.1 Mbps (Efficiency 70.01%)
  - Support STBC, LDPC, TX beamformee and beamformer
  - Greenfield, mixed mode, legacy modes support
  - IEEE 802.11 d/e/h/i/j/k/mc/r/v/w support
  - Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
  - QoS support of WFA WMM, WMM PS
  - Integrated LNA, PA, and T/R switch
  - Optional external LNA and PA support.

1.3 Wired Ethernet Features

- **Frame Engine**
  - Packet DMA (PDMA)
    - 4 Tx descriptor and 4 Rx descriptor rings
    - Scattter/Gather DMA
    - Configurable 4/8/16/32 32-bit burst legnth and delayed interrupt
    - Support LRO and TSO
  - QoS DMA (QDMA)
    - Supports 64 Tx queues
    - Per Tx queue forward/drop packet accounting
    - Per Tx queue forward byte accounting
    - Per Tx queue min/max rate control
    - Supports up to 1024 virtual queues
  - WiFi Warp Drive (WWD)
    - Ethernet to WiFi offlaod, forwarding packet directly
    - PCIe Interrupt interception and proxy
    - Dynamic buffer allocate and release
  - Packet Switch Engine (PSE)
    - 1000Mbps wire-speed NAT/NAPT routing
    - Egress rate limiting/shaping
    - IP/TCP/UDP checksum offload
    - IP/TCP/UDP checksum generation
    - VLAN & PPPoE header insertion
    - TCP segmentation offload
  - Packet Process Engine (PPE)
    - IPv4 NAP/NAPT, IPv6 Routing and Tunnel IP (DS-Lite, 6RD)
    - 1/24/8/16K session/flow
    - Stateful packet filtering (SPI)
    - Patent-pending flow offloading technology for flexible/high performance packet L3/L4 packet processing.
    - Support NAT/NAPT up to 3.5Gbps wire-speed within 32 flows for any packet size.

  (note): All PPE features mentioned above require software porting to function.

- **Fast Ethernet Switch**
  - Embedded 5-ports 10/100Mbps PHY
  - Support Spanning Tree Port states
  - Support 1K-MAC address table with direct or XOR hash
  - QoS
    - Four priorities queues per port
    - Packet classification based on incoming port, IEEE 802.1p or IP ToS/DSCP
    - Strict-Priority Queue (PQ) and Weighted Round Robin (WRR)
  - VLAN
    - Port Base VLAN
    - Double VLAN tagging
    - 802.1q tag VLAN
    - 16 VIDs
  - MAC address table read and write-able

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- MAC security – Locking a MAC address to an incoming port
- MAC clone support – hash with VID
- IGMP and MLD support
- Per-Port Broadcast storm prevention

- **GigaMAC (GMAC)**
  - Support IEEE 802.3x full duplex flow control
  - Support MII/revMII/RGMII/SGMII interface
  - SGMII supports 10/100/1000Mbps speed change through auto-negotiation and configurable 2.5Gbps SerDes link.

1.4 Main Features Summary

The following table covers the main features offered by MT7622B. Overall,

Table 1-1 Main Features

Features	MT7622B
CPU	ARM CA53 (1.35GHz, Dual-core), NEON
I-Cache, D-Cache	32kB, 32kB per core
L2 Cache	512KB
Security	CA53 crypto extension instruction ARM Trust Zone Support 4* 256-bit Multi-key on OTP efuse Support 128-bit OTP efuse for Anti-roll back
IO Coherence	MCI (MTK patent pending)
DRAM data	16bit
DDR2	1066 Mbps (max 1Gb)
DDR3	1600 Mbps (max 8Gb by 16-bit and 16Gb by 8-bit)
WIFI	2x2 11n 2.4GHz (256QAM) Integrated PA, LNA and TR-SW 5/10/20/40MHz bandwidth Support 256QAM Support external LNA and PA support (option)
Ethernet	5-port 10/100Mbps ESW RGMII x 1 (H)SGMII x 1
HNAT/HQoS	HQoS 64 queues, SFQ 1K queues HNAT 3.5Gbps forwarding (IPv4, IPv6 routing, DS-Lite, 6RD, 6to4)

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Features	MT7622B
WIFI Wrap Drive (w/. MT7615)	Ethernet to WiFi HNAT to offload CPU PCIe Interrupt interception and proxy
PCIe	PCIe2.0 x 2 (2nd port pin sharing w/ SATA) or 2-lane x 1
SATA	SATA3.0 x 1 (pin sharing w/. 2nd PCIe) Support eSATA up to Gen 2
USB	USB2.0 Host x 1 USB3.0 x 1
SD eMMC	SD3.0 SDR104 w/. 4-bit eMMC4.4.1
NAND Flash	SLC NAND interface supports 8-pin I/O ECC (BCH code) acceleration capable of 16-bit error correction (w/. ECC engine) Provides SPI NAND flash interface (*note) SLC NAND pin sharing w/ eMMC4.4.1.
SPI Flash (NOR)	Max 50MHz data bit width x1/x2/x4 Support 4-byte address mode compatible with 3-byte address mode
I2C	I2C x 3 Max 400kHz Support 7/10-bit addressing
SPI	SPI x 2 Support DMA and FIFO mode
UART	UART-Lite(2-pins) x 1 UART(4-pins) x 4 Support both M16C450 and M16550 modes of operation
Package	FCCSP 15 x 15 mm

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2 Pins

2.1 Ball Map (Top View)

Table 2-1 Ball Map (Left-Side)

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC1	AVDD13_WF0_SX	AVDD13_WF0_AFE	XO	AVDD22_XO	AVDD22_BT	NC5	GND_RF	PWM7			SPIC1_CS
B	AVDD13_WF0_TRX	AVDD22_WF0	AVDD22_WF0_BBPLL	GND_RF	GND_RF		AVDD33_BT	GND_RF	PWM6		PWM1	SPIC1_CLK
C	WF0_RXG_LNA_IN	GND_RF	GND_RF	WF0_VCO_MON	GND_RF	GND_RF	AVDD13_BT	GND_RF	PWM5	PWM4	PWM2	GPIO_D
D		WF0_RFIO_G	GND_RF	GND_RF	GND_RF	GND_RF			RXD4	DVDD18_IO3	DVDD28_IO3	
E	AVDD33_WF0_PA	AVDD33_WF0_PA	GND_RF	AVDD13_WF1_TRX	GND_RF	GND_RF	GND_RF				PERST1_N	GND
F		WF1_RXG_LNA_IN	GND_RF	GND_RF		GND_RF	GND_RF	EPHY_LED0_N	TXD4	CTS4_N	TXD3	AVDD18_PLLGP
G		WF1_RFIO_G	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	WLED_N	RTS4_N		PWM3
H	AVDD33_WF1_PA	AVDD33_WF1_PA	AVDD13_WF2_TRX	GND_RF	GND_RF	GND_RF	GND_RF	GND	VCCK	VCCK	VCCK_VSRAM	VCCK
J		WF2_RXG_LNA_IN	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND	VCCK	VCCK	GND	VCCK
K		WF2_RFIO_G	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND	VCCK	VCCK	GND	VPROC
L	AVDD33_WF2_PA	AVDD33_WF2_PA	AVDD13_WF3_TRX	GND_RF	GND_RF	GND_RF	GND_RF	GND	VCCK	VCCK	GND	VPROC
M		WF3_RXG_LNA_IN	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND	VCCK	VCCK	GND	VPROC
N		WF3_RFIO_G	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND	VCCK	VCCK	GND	VPROC
P	AVDD33_WF3_PA	AVDD33_WF3_PA	AVDD22_WF3	GND_RF		GND	GND	GND	VCCK	VCCK	GND	GND
R	AVDD13_WF3_AFE	GND_RF	GND_RF	GND_RF	GND	GND	GND	GND	GND	VCCK_VSRAM	GND	GND
T	GND_RF	GND_RF	GPIO_A	TXD0	AVDD33_TX	AVDD33_TX	GND	GND	GND		DVDD28_IO1	
U	I2S_MCLK	I2S1_IN	I2S1_OUT	RXD0				SPI_MOSI	SPI_CS	SPI_MISO	GPIO_B	DVDD28_IO2
V		I2S_WS	I2S_BCLK	I2C_SCL	I2C_SDA	I2S4_IN	I2S4_OUT			SPI_CLK	SPI_WP	
W	GND	EPHY_VRT	AVDD18_EPHY	GND	I2S2_OUT	I2S3_OUT				GND	SPI_HOLD	
Y	MDI_RP_P0	MDI_RN_P0	AVDD33_TXP0		I2S2_IN	I2S3_IN						GND
AA	MDI_TP_P0	MDI_TN_P0	MDI_RN_P1		MDI_TN_P2	MDI_RP_P3	MDI_RP_P4	MDI_TN_P4	G2_TXD3	G2_TXD0	GND	G2_RXC
AB	MDI_TP_P1	MDI_TN_P1	MDI_RN_P2	MDI_TP_P2	MDI_TP_P3	MDI_RN_P3	MDI_RN_P4	GND	G2_TXD2	G2_TXEN	G2_TXC	
AC	NC2	MDI_RP_P1	MDI_RP_P2		MDI_TN_P3		MDI_TP_P4		G2_TXD1		GND	
	1	2	3	4	5	6	7	8	9	10	11	12

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Table 2-2 Ball Map (Right-Side)

13	14	15	16	17	18	19	20	21	22	23	
PERST0_N	WATCHDOG		AVDD18_RTC			PCIE1_TXP	GND	PCIE0_RXN	PCIE0_RXP	NC4	A
GPIO_E	AUXIN0	AUXIN1	NC6		PCIE1_RXP	GND	PCIE1_TXN	AVDD18_PCIE	GND	PCIE0_TXN	B
RXD3	AUXIN2	AUXIN3		NC7	AVDD10_PCIE0	PCIE1_RXN		PCIE0_CLKN	GND	PCIE0_TXP	C
RTS3_N	SPIC1_MISO		SPIC1_MOSI		PCIE1_CLKN	AVDD10_PCIE1	PCIE0_CLKP	GND	GND		D
		GND	SYSRSTB	GND	PCIE1_CLKP		GND	RBA0	RA7	RA13	E
AVSS18_AP		AVDD18_AP	DVDD18_IO4	GND	GND	RCLK0_	RCLK0	RA2	RA9		F
AVSS18_PLLGP		AVDD33_PMU	CTS3_N	TESTMODE		GND		RA15	RBA2	RA0	G
VCCK	DDRVCCIO_CLK	PMIC_SDA	PMIC_SCL	RCS_	RA5	RCKE		RA12			H
VPROC	DDRVCCIO	DDRVCCIO	TP_MEMPLL		DDR3RSTB	RODT_	RA1	RA11	RA14		J
VPROC	VCCK	GND	AVSS18_MEMPLL	GND	GND	RA3	RWE_	RA6	RA8	GND	K
VPROC	GND	DDRVCCIO		AVDD18_MEMPLL	RCAS_		GND	RBA1	RA4		L
VPROC	GND	DDRVCCIO	GND	RDQM1	RRAS_	RA10	GND	RDQ7		GND	M
VPROC	GND	DDRVCCIO	GND	RDQS1	RDQS1_	GND	RDQ3	RDQ5	RDQ1		N
VPROC	GND	GND	GND	GND		GND	GND	RDQ12	RDQ14		P
VPROC	GND	VPROC_VSRAM	GND	GND	RDQS0	RDQS0_	RVREF	RDQ10		GND	R
		DVDD18_IO1	GND	GND	GND	RDQM0	GND	RDQ8	RDQ11	RDQ9	T
							GND	RDQ15	RDQ13		U
DVDD18_IO2		NCEB	NCLE	NALE	NWEB			RDQ0			V
	MDIO	NDL3	NDL2	NDL1	NDL0		REXTDN	RDQ2	RDQ6	RDQ4	W
G2_RXD2	MDC	NDL7		NDL6	NDL5	NDL4	NREB	NRB			Y
G2_RXDV	G2_RXD3	GND	SGMII_RXN					GND	USB_DM_P1	USB_DP_P1	AA
G2_RXD0		SGMII_TXN	SGMII_RXP	GND	SSUSB_TXP	GND	SSUSB_RXP	AVDD33_USB	USB_DM_P0	USB_DP_P0	AB
G2_RXD1		SGMII_TXP		AVDD10_SGMII	AVDD10_SSUSB	SSUSB_TXN	AVDD18_SGMII_SSUSB	SSUSB_RXN	AVDD18_USB	NC3	AC
13	14	15	16	17	18	19	20	21	22	23	

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2.2 Pin Descriptions

Table 2-3 Pin Description

Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Pull	State *1	Aux *2	Pull				
GPIO										
T3	GPIO_A	I	-	I/O	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO
U11	GPIO_B	I	-	I/O	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO
C12	GPIO_D	I	-	I/O	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO
B13	GPIO_E	I	-	I/O	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO
UART										
T4	TXD0	I	PD	O	0	-	PU/PD	3.3	4/8/12/16	UART TX data
U4	RXD0	I	-	I	0	-	PU/PD	3.3	4/8/12/16	UART RX data
F11	TXD3	I	-	O	0	-	PU/PD	3.3	4/8/12/16	UART TX data
C13	RXD3	I	-	I	0	-	PU/PD	3.3	4/8/12/16	UART RX data
G16	CTS3_N	I	-	I	0	-	PU/PD	3.3	4/8/12/16	UART clear to send
D13	RTS3_N	I	-	O	0	-	PU/PD	3.3	4/8/12/16	UART request to send
F9	TXD4	I	-	O	0	-	PU/PD	3.3	4/8/12/16	UART TX data
D9	RXD4	I	-	I	0	-	PU/PD	3.3	4/8/12/16	UART RX data
F10	CTS4_N	I	-	I	0	-	PU/PD	3.3	4/8/12/16	UART clear to send
G10	RTS4_N	I	-	O	0	-	PU/PD	3.3	4/8/12/16	UART request to send
I2C										
V5	I2C_SDA	I	-	OD	0	-	PU/PD	3.3	4/8/12/16	I2C Serial Clock
V4	I2C_SCL	I	-	OD	0	-	PU/PD	3.3	4/8/12/16	I2C Serial Data
SPI										
B12	SPIC1_CLK	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Serial Peripheral Interface Serial Clock
D16	SPIC1_MOSI	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Serial Peripheral Interface Master Output, Slave Input
D14	SPIC1_MISO	I	-	I	0	-	PU/PD	3.3	4/8/12/16	Serial Peripheral Interface Master Input, Slave Output
A12	SPIC1_CS	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Serial Peripheral Interface Slave Select
PWM										
B11	PWM1	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Pulse width modulator
C11	PWM2	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Pulse width modulator
G12	PWM3	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Pulse width modulator
C10	PWM4	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Pulse width modulator
C9	PWM5	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Pulse width modulator
B9	PWM6	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Pulse width modulator
A9	PWM7	I	-	I/O	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Pull	State *1	Aux *2	Pull				
SFlash										
V11	SPI_WP	I		I/O	0		PU/PD	3.3	4/8/12/16	Serial Flash Write Protect
W11	SPI_HOLD	I		I/O	0		PU/PD	3.3	4/8/12/16	Serial Flash HOLD
V10	SPI_CLK	I		O	0		PU/PD	3.3	4/8/12/16	Serial Flash Clock
U8	SPI_MOSI	I		I/O	0		PU/PD	3.3	4/8/12/16	Serial Flash Master Output, Slave Input
U10	SPI_MISO	I		I/O	0		PU/PD	3.3	4/8/12/16	Serial Flash Master Input, Slave Output
U9	SPI_CS	I		O	0		PU/PD	3.3	4/8/12/16	Serial Flash Chip Select
NAND										
V15	NCEB	I	-	O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Chip Select
V18	NWEB	I	PD	O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Write Enable
V16	NCLE	I	PD	O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Command Latch Enable
V17	NALE	I	PD	O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Address Latch Enable
Y21	NRB	I	-	I	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Ready Busy
Y20	NREB	I	PD	O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Read Enable
W18	NDL0	I	-	I/O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Data Bus bit0
W17	NDL1	I	-	I/O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Data Bus bit1
W16	NDL2	I	-	I/O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Data Bus bit2
W15	NDL3	I	-	I/O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Data Bus bit3
Y19	NDL4	I	-	I/O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Data Bus bit4
Y18	NDL5	I	-	I/O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Data Bus bit5
Y17	NDL6	I	-	I/O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Data Bus bit6
Y15	NDL7	I	-	I/O	0	-	PU/PD	1.8	4/8/12/16	NAND Flash Data Bus bit7
RGMII										
AA12	G2_RXC	I	-	I	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII RX clock
AA13	G2_RXDV	I	-	I	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII RX data valid
AB13	G2_RXD0	I	-	I	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII RX data bit #0
AC13	G2_RXD1	I	-	I	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII RX data bit #1
Y13	G2_RXD2	I	-	I	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII RX data bit #2
AA14	G2_RXD3	I	-	I	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII RX data bit #3
AB11	G2_TXC	I	-	O	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII TX clock
AB10	G2_TXEN	I	-	O	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII TX data valid
AA10	G2_TXD0	I	-	O	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII TX data bit #0
AC9	G2_TXD1	I	-	O	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII TX data bit #1
AB9	G2_TXD2	I	-	O	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII TX data bit #2
AA9	G2_TXD3	I	-	O	0	-	PU/PD	2.5/3.3	4/8/12/16	GE2 RGMII TX data bit #3

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Pull	State *1	Aux *2	Pull				
SM										
Y14	MDC	I	PD	O	0	PD	PU/PD	3.3	4/8/12/16	Serial management clock
W14	MDIO	I		I/O	0		PU/PD	3.3	4/8/12/16	Serial management data
I2S										
U1	I2S_MCLK	I		O	0	PD	PU/PD	3.3	4/8/12/16	General Purpose IO
V3	I2S_BCLK	I		O	0	PD	PU/PD	3.3	4/8/12/16	General Purpose IO
V2	I2S_WS	I		O	0	PD	PU/PD	3.3	4/8/12/16	General Purpose IO
U2	I2S1_IN	I		I	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO
Y5	I2S2_IN	I		I	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO
Y6	I2S3_IN	I		I	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO
V6	I2S4_IN	I		I	0	-	PU/PD	3.3	4/8/12/16	General Purpose IO
U3	I2S1_OUT	I		O	0	PD	PU/PD	3.3	4/8/12/16	General Purpose IO
W5	I2S2_OUT	I		O	0	PD	PU/PD	3.3	4/8/12/16	General Purpose IO
W6	I2S3_OUT	I		O	0	PD	PU/PD	3.3	4/8/12/16	General Purpose IO
V7	I2S4_OUT	I		O	0	PD	PU/PD	3.3	4/8/12/16	General Purpose IO
LED										
F8	EPHY_LED0_N	I		O	0		PU/PD	3.3	4/8/12/16	ESW Port #0 LED
G9	WLED_N	I		O	0		PU/PD	3.3	4/8/12/16	WLAN LED
ESW										
W2	EPHY_VRT	A		A				3.3		Band gap resistor which is connected to AVSS33 through a 24kΩ (±1%) resistor
AA1	MDI_TP_P0	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #0 MDI Transceivers (5Kohm +-20% pull-down)
AA2	MDI_TN_P0	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #0 MDI Transceivers (5Kohm +-20% pull-down)
Y1	MDI_RP_P0	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #0 MDI Transceivers (5Kohm +-20% pull-down)
Y2	MDI_RN_P0	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #0 MDI Transceivers (5Kohm +-20% pull-down)
AB1	MDI_TP_P1	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #1 MDI Transceivers (5Kohm +-20% pull-down)
AB2	MDI_TN_P1	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #1 MDI Transceivers (5Kohm +-20% pull-down)
AC2	MDI_RP_P1	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #1 MDI Transceivers (5Kohm +-20% pull-down)
AA3	MDI_RN_P1	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #1 MDI Transceivers (5Kohm +-20% pull-down)
AB4	MDI_TP_P2	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #2 MDI Transceivers (5Kohm +-20% pull-down)

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Pull	State *1	Aux *2	Pull				
AA5	MDI_TN_P2	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #2 MDI Transceivers (5Kohm +-20% pull-down)
AC3	MDI_RP_P2	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #2 MDI Transceivers (5Kohm +-20% pull-down)
AB3	MDI_RN_P2	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #2 MDI Transceivers (5Kohm +-20% pull-down)
AB5	MDI_TP_P3	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #3 MDI Transceivers (5Kohm +-20% pull-down)
AC5	MDI_TN_P3	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #3 MDI Transceivers (5Kohm +-20% pull-down)
AA6	MDI_RP_P3	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #3 MDI Transceivers (5Kohm +-20% pull-down)
AB6	MDI_RN_P3	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #3 MDI Transceivers (5Kohm +-20% pull-down)
AC7	MDI_TP_P4	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #4 MDI Transceivers (5Kohm +-20% pull-down)
AA8	MDI_TN_P4	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #4 MDI Transceivers (5Kohm +-20% pull-down)
AA7	MDI_RP_P4	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #4 MDI Transceivers (5Kohm +-20% pull-down)
AB7	MDI_RN_P4	A	PD	A	PD			3.3	4/8/12/16 (*5)	Port #4 MDI Transceivers (5Kohm +-20% pull-down)
SGMII										
AB15	SGMII_TXN	A		A				3.3		SGMII differential transmit TX -
AC15	SGMII_TXP	A		A				3.3		SGMII differential transmit TX+
AA16	SGMII_RXN	A		A				3.3		SGMII differential receive RX -
AB16	SGMII_RXP	A		A				3.3		SGMII differential receive RX +
PCIe										
C21	PCIE0_CLKN	A		A				3.3		PCIe port0 reference clock (negative)
D20	PCIE0_CLKP	A		A				3.3		PCIe port0 reference clock (positive)
B23	PCIE0_TXN	A		A				3.3		PCIe port0 differential transmit TX -
C23	PCIE0_TXP	A		A				3.3		PCIe port0 differential transmit TX+
A21	PCIE0_RXN	A		A				3.3		PCIe port0 differential receive RX -
A22	PCIE0_RXP	A		A				3.3		PCIe port0 differential receive RX +
D18	PCIE1_CLKN	A		A				3.3		PCIe port1 reference clock (negative)

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description	
		State *1	Pull	State *1	Aux *2	Pull					
E18	PCIE1_CLKP	A		A				3.3		PCIe port1 reference clock (positive)	
B20	PCIE1_TXN	A		A				3.3		PCIe port1 differential transmit TX -	
A19	PCIE1_TXP	A		A				3.3		PCIe port1 differential transmit TX+	
C19	PCIE1_RXN	A		A				3.3		PCIe port1 differential receive RX -	
B18	PCIE1_RXP	A		A				3.3		PCIe port1 differential receive RX +	
USB											
AB22	USB_DM_P0	A		A				3.3		USB port0 HS/FS/LS data pin Data- (USB2.0)	
AB23	USB_DP_P0	A		A				3.3		USB port0 HS/FS/LS data pin Data+ (USB2.0)	
AA22	USB_DM_P1	A		A				3.3		USB port1 HS/FS/LS data pin Data- (USB3.0)	
AA23	USB_DP_P1	A		A				3.3		USB port1 HS/FS/LS data pin Data+ (USB3.0)	
AC21	SSUSB_RXN	A		A				3.3		SSUSB data pin RX- (USB3.0)	
AB20	SSUSB_RXP	A		A				3.3		SSUSB data pin RX+ (USB3.0)	
AC19	SSUSB_TXN	A		A				3.3		SSUSB data pin TX- (USB3.0)	
AB18	SSUSB_TXP	A		A				3.3		SSUSB data pin TX+ (USB3.0)	
DDR										**DDR2 (1.8V)**	**DDR3 (1.5/1.35V)**
V21	RDQ0	I/O		I/O						Data bit #6	Data bit #0
N22	RDQ1	I/O		I/O						Data bit #2	Data bit #1
W21	RDQ2	I/O		I/O						Data bit #1	Data bit #2
N20	RDQ3	I/O		I/O						Data bit #0	Data bit #3
W23	RDQ4	I/O		I/O						Data bit #4	Data bit #4
N21	RDQ5	I/O		I/O						Data bit #7	Data bit #5
W22	RDQ6	I/O		I/O						Data bit #3	Data bit #6
M21	RDQ7	I/O		I/O						Data bit #5	Data bit #7
T21	RDQ8	I/O		I/O						Data bit #14	Data bit #8
T23	RDQ9	I/O		I/O						Data bit #10	Data bit #9
R21	RDQ10	I/O		I/O						Data bit #8	Data bit #10
T22	RDQ11	I/O		I/O						Data bit #9	Data bit #11
P21	RDQ12	I/O		I/O						Data bit #15	Data bit #12
U22	RDQ13	I/O		I/O						Data bit #11	Data bit #13
P22	RDQ14	I/O		I/O						Data bit #13	Data bit #14
U21	RDQ15	I/O		I/O						Data bit #12	Data bit #15

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description	
		State *1	Pull	State *1	Aux *2	Pull					
G23	RA0	O		O						Address bit #5	Address bit #0
J20	RA1	O		O						Address bit #11	Address bit #1
F21	RA2	O		O						Address bit #9	Address bit #2
K19	RA3	O		O							Address bit #3
L22	RA4	O		O						Address bit #2	Address bit #4
H18	RA5	O		O						Address bit #10	Address bit #5
K21	RA6	O		O						Address bit #4	Address bit #6
E22	RA7	O		O						Address bit #7	Address bit #7
K22	RA8	O		O						Address bit #6	Address bit #8
F22	RA9	O		O						Address bit #12	Address bit #9
M19	RA10	O		O						RRAS	Address bit #10
J21	RA11	O		O						Address bit #8	Address bit #11
H21	RA12	O		O						RWE	Address bit #12
E23	RA13	O		O						Address bit #3	Address bit #13
J22	RA14	O		O						Address bit #13	Address bit #14
G21	RA15	O		O						Bank Address #1	Address bit #15
E21	RBA0	O		O							Bank Address #0
L21	RBA1	O		O						Address bit #0	Bank Address #1
G22	RBA2	O		O						Address bit #1	Bank Address #2
M18	RRAS_	O		O						Bank Address #2	RAS
L18	RCAS_	O		O						Bank Address #0	CAS
K20	RWE_	O		O						RCAS	RWE
F20	RCLK0	O		O						Clock 0+	Clock 0+
F19	RCLK0_	O		O						Clock 0-	Clock 0-
T19	RDQM0	O		O						DQM#0	DQM#0
M17	RDQM1	O		O						DQM#1	DQM#1
H17	RCS_	O		O						RCS	RCS
R18	RDQS0	I/O		I/O						DQS 0+	DQS 0+
R19	RDQS0_	I/O		I/O						DQS 0-	DQS 0-
N17	RDQS1	I/O		I/O						DQS 1+	DQS 1+
N18	RDQS1_	I/O		I/O						DQS 1-	DQS 1-
H19	RCKE	O		O						CKE	CKE
J18	DDR3RSTB	O		O							DDR3RSTB
J19	RODT	O		O						RODT	RODT

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description	
		State *1	Pull	State *1	Aux *2	Pull					
R20	RVREF	O		O				0.75 0.675 0.6		DRAM reference voltage power supply	DRAM reference voltage power supply
W20	REXTDN	O		O						Output Driving Calibration	Output Driving Calibration
J16	TP_MEMPL	O		O						TP	TP
WIFI											
N2	WF3_RFIO_G	A		A						WF3 TX Output	
M2	WF3_RXG_LNA_IN	A		A						WF3 RX Input	
K2	WF2_RFIO_G	A		A						WF2 TX Output	
J2	WF2_RXG_LNA_IN	A		A						WF2 RX Input	
G2	WF1_RFIO_G	A		A						WF1 TX Output	
F2	WF1_RXG_LNA_IN	A		A						WF1 RX Input	
D2	WF0_RFIO_G	A		A						WF0 TX Output	
C1	WF0_RXG_LNA_IN	A		A						WF0 RX Input	
C4	WF0_VCO_MON	A		A						WF RF Test Pin	
A4	XO	A		A						25MHz Clock Source	
A7	NC5									NC	
PMIC											
H15	PMIC_SDA	I		I/O	0		PU/PD	1.8	4/8/12/16	PMIC SPI data	
H16	PMIC_SCL	I	PD	O	0	PD	PU/PD	1.8	4/8/12/16	PMIC SPI clock	
NC											
B16	NC6	A		A				1.8		NC	
C17	NC7	A		A				1.8		NC	
GPIO											
B14	AUXIN0	A		A		-	PU/PD	1.8		General Purpose IO	
B15	AUXIN1	A		A		-	PU/PD	1.8		General Purpose IO	
C14	AUXIN2	I	-	IO	0	-	PU/PD	1.8		General Purpose IO	
C15	AUXIN3	I	-	IO	0	-	PU/PD	1.8		General Purpose IO	
MISC											
E16	SYSRSTB	I	PU	I	-	PU	PU	1.8	-	Power-on Reset	
G17	TESTMODE	I	PD	I	-	PD	PD	1.8	-	Test Mode	
A14	WATCHDOG	I	-	O	0	-	PU/PD	3.3	4/8/12/16	Watchdog Reset	
A13	PERST0_N	I	-	O	0	-	PU/PD	3.3	4/8/12/16	PCIe Reset	
E11	PERST1_N	I	-	O	0	-	PU/PD	3.3	4/8/12/16	PCIe Reset	
A1, A23, AC1, AC23	NC1 NC2 NC3 NC4	NC	-	NC	-	-	-			NC	

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Pull	State *1	Aux *2	Pull				
POWER										
H9, H10, H12, H13, J9, J10, J12, K9, K10, K14, L9, L10, M9, M10, N9, N10, P9, P10,	VCCK	P		P				1.15		Digital core power supply
H11, R10	VCCK_SRAM	P		P				1.15		Core SRAM power supply
J13, K12, K13, L12, L13, M12, M13, N12, N13, P13, R13	VPROC	P		P				0.95 1.0 1.05 1.1 1.15 1.2 1.25 1.35		CPU core power supply
R15	VPROC_SRAM	P		P				1.15 1.2 1.25 1.3 1.35		CPU SRAM power supply
J14, J15, L15, M15, N15	DDRVCCIO	P		P				1.8 1.5 1.35		DDR I/O power supply
H14	DDRVCCIO_CLK	P		P				1.8 1.5 1.35		DDR CLK power supply
T15	DVDD18_IO1	P		P				1.8		Digital I/O power supply
V13	DVDD18_IO2	P		P				1.8		Digital I/O power supply
D10	DVDD18_IO3	P		P				1.8		Digital I/O power supply
F16	DVDD18_IO4	P		P				1.8		Digital I/O power supply
T11	DVDD28_IO1	P		P				3.3		Digital I/O power supply
U12	DVDD28_IO2	P		P				2.5 3.3		Digital I/O power supply (RGMII)
D11	DVDD28_IO3	P		P				3.3		Digital I/O power supply
D19	AVDD10_PCIE1	P		P				1.15		PCIE1 analog power supply
AC17	AVDD10_SGMII	P		P				1.15		SGMII analog power supply
AC18	AVDD10_SSUSB	P		P				1.15		SSUSB analog power supply
C18	AVDD10_PCIE0	P		P				1.15		PCIE0 analog power supply
A2	AVDD13_WF0_SX	P		P				1.15		WF0 analog power supply
C7	AVDD13_BT	P		P				1.15		analog power supply

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Pull	State *1	Aux *2	Pull				
A3	AVDD13_WF0_AFE	P		P				1.15		WF0 analog power supply
R1	AVDD13_WF3_AFE	P		P				1.15		WF3 analog power supply
B1	AVDD13_WF0_TRX	P		P				1.15		WF0 analog power supply
E4	AVDD13_WF1_TRX	P		P				1.15		WF1 analog power supply
H3	AVDD13_WF2_TRX	P		P				1.15		WF2 analog power supply
L3	AVDD13_WF3_TRX	P		P				1.15		WF3 analog power supply
F15	AVDD18_AP	P		P				1.8		ADC analog power supply
L17	AVDD18_MEMPLL	P		P				1.8		DRAM PLL power supply
B21	AVDD18_PCIE	P		P				1.8		PCIE analog power supply
F12	AVDD18_PLLGP	P		P				1.8		PLL group analog power supply
AC20	AVDD18_SGMII_SSUSB	P		P				1.8		SGMII/SSUSB analog power supply
AC22	AVDD18_USB	P		P				1.8		USB analog power supply
W3	AVDD18_EPHY	P		P				1.8		EPHY analog power supply
A16	AVDD18_RTC	P		P				1.8		analog power supply
A5	AVDD22_XO	P		P				2.2		RF XTAL analog power supply
A6	AVDD22_BT	P		P				2.2		analog power supply
B3	AVDD22_WF0_BBPLL	P		P				2.2		WF BBPLL analog power supply
B2	AVDD22_WF0	P		P				2.2		WF0 analog power supply
P3	AVDD22_WF3	P		P				2.2		WF3 analog power supply
E1, E2	AVDD33_WF0_PA	P		P				3.3		WF0 PA analog power supply
H1, H2	AVDD33_WF1_PA	P		P				3.3		WF1 PA analog power supply
L1, L2	AVDD33_WF2_PA	P		P				3.3		WF2 PA analog power supply
P1, P2	AVDD33_WF3_PA	P		P				3.3		WF3 PA analog power supply
T5, T6	AVDD33_TX	P		P				3.3		EPHY TX analog power supply
B7	AVDD33_BT	P		P				3.3		analog power supply
G15	AVDD33_PMU	P		P				3.3		PMU analog power supply
AB21	AVDD33_USB	P		P				3.3		USB analog power supply
Y3	AVDD33_TXP0	P		P				3.3		EPHY P0 analog power supply
GROUND										
F13	AVSS18_AP	G		G						Ground for ADC
G13	AVSS18_PLLGP	G		G						Ground for PLL
K16	AVSS18_MEMPLL	G		G						Ground for MEMPLL

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Pull	State *1	Aux *2	Pull				
A8, B4, B5, B8, C2, C3, C5, C6, C8, D3, D4, D5, D6, E3, E5, E6, E7, F3, F4, F6, F7, G3, G4, G5, G6, G7, G8, H4, H5, H6, H7, J3, J4, J5, J6, J7, K3, K4, K5, K6, K7, L4, L5, L6, L7, M3, M4, M5, M6, M7, N3, N4, N5, N6, N7, P4, R2, R3, R4, T1, T2,	GND_RF	G		G						RF Ground

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Pin	Name	Reset		After Reset			PU/PD *3,4	Voltage (V)	Driving (mA)	Description
		State *1	Pull	State *1	Aux *2	Pull				
A20, B19, B22,C22,D21,D22, E12, E15, E17, E20, F17, F18, G19, H8, J8, J11, K8, K11, K15, K17, K18, K23, L8, L11, L14, L20, M8, M11, M14,M16, M20,M23, N8, N11, N14, N16, N19, P6, P7, P8, P11, P12, P14, P15, P16, P17, P19, P20, R5, R6, R7, R8, R9, R11, R12, R14, R16, R17, R23, T7, T8, T9, T16, T17, T18, T20, U20, W1, W4, W10, Y12, AA11, AA15, AA21, AB8, AB17, AB19, AC11	GND	G		G						Ground

NOTE:

1. I: Input
   O: Output
   I/O: Bi-directional
   P: Power
   G: Ground
   NC: Not connected
   A: Analog
2. Please refer to section 2.3 for pin aux. function
3. The internal pull resistance value is 75 kΩ.
4. PD: Internal pull-down
   PU: Internal pull-up
   NP: No pull-down/up

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5. Digital GPIO drive capability (5K ohm pull-down ressitor still exist when IO is switched to the digital GPIO)

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2.2.1 Constant Tie Pins

Table 2-4 Constant tied pins

Pin name	Description
TESTMODE	Test mode (tie to GND)

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2.3 Pin Sharing Schemes

Some pins are shared with GPIO to provide maximum flexibility for system designers. The MT7622B provides up to 102 GPIO pins. Users can configure registers specify the pin function. For more information, see the Programmer's Guide. The pin's default function mode is configured on Func.0.

2.3.1 Pin share scheme

Table 2-5 Pin Share

Pin	Func. 0	Func. 1	Func. 2	Func. 3	Func. 4	Func. 5	Func. 6	Func. 7
MDI_TP_P0	TXD2 (O)	GPIO51		PWM_CH1 (O)				
MDI_TN_P0	RXD2 (I)	GPIO52		PWM_CH2 (O)				
MDI_RP_P0	RTS2_N (O)	GPIO53		PWM_CH3 (O)				
MDI_RN_P0	CTS2_N (I)	GPIO54		PWM_CH4 (O)				
MDI_TP_P1	I2C1_SCL (IO)	GPIO55	TXD1 (O)					
MDI_TN_P1	I2C1_SDA (IO)	GPIO56	RXD1 (I)					
MDI_RP_P1	I2C2_SCL (IO)	GPIO57	RTS1_N (O)			TXD3 (O)		
MDI_RN_P1	I2C2_SDA (IO)	GPIO58	CTS1_N (I)			RXD3 (I)		
MDI_RP_P2		GPIO59			TXD2 (O)			
MDI_RN_P2		GPIO60			RXD2 (I)			
MDI_TP_P2		GPIO61			RTS2_N (O)	TXD4 (O)		
MDI_TN_P2		GPIO62			CTS2_N (I)	RXD4 (I)		
MDI_TP_P3		GPIO63			SPIC0_CLK (O)			
MDI_TN_P3		GPIO64			SPIC0_MOSI (O)			
MDI_RP_P3		GPIO65			SPIC0_MISO (I)			
MDI_RN_P3		GPIO66			SPIC0_CS (O)			
MDI_RP_P4		GPIO67		PWM_CH4 (O)	SPIC1_CLK (O)			
MDI_RN_P4		GPIO68		PWM_CH5 (O)	SPIC1_MOSI (O)			
MDI_TP_P4		GPIO69		PWM_CH6 (O)	SPIC1_MISO (I)			
MDI_TN_P4		GPIO70			SPIC1_CS (O)			
GPIO_A	GPIO (IO)	GPIO0						
I2S1_IN		GPIO1	RTS2_N (O)					
I2S1_OUT		GPIO2	CTS2_N (I)					
I2S_BCLK		GPIO3	TXD2 (O)					

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I2S_WS		GPIO4	RXD2 (I)					
I2S_MCLK		GPIO5						DBG_UTIF[17] (IO)
TXD0	TXD0 (O)	GPIO6						TM_SUTIF_TXD (O)
RXD0	RXD0 (I)	GPIO7						TM_SUTIF_RXD (I)
SPI_WP	SPI_WP (IO)	GPIO8	SNFI_WP (IO)					
SPI_HOLD	SPI_HOLD (IO)	GPIO9	SNFI_HOLD (IO)					
SPI_CLK	SPI_CLK (O)	GPIO10	SNFI_CLK (O)					
SPI_MOSI	SPI_MOSI (IO)	GPIO11	SNFI_MOSI (IO)					
SPI_MISO	SPI_MISO (IO)	GPIO12	SNFI_MISO (IO)					
SPI_CS	SPI_CS (O)	GPIO13	SNFI_CS (O)					
I2C_SDA	I2C0_SDA (IO)	GPIO14	PCIE0_PAD_WAKE_N (IO)	PCIE1_PAD_WAKE_N (IO)		ANTSEL[22] (O)		TM_EXT_BGCK (I)
I2C_SCL	I2C0_SCL (IO)	GPIO15	PCIE0_PAD_CLKREQ_N (IO)	PCIE1_PAD_CLKREQ_N (IO)		ANTSEL[23] (O)		
I2S2_IN		GPIO16	SD_D3 (IO)			ANTSEL[24] (O)		DBG_UTIF[10] (IO)
I2S3_IN		GPIO17	SD_D2 (IO)			ANTSEL[25] (O)		DBG_UTIF[11] (IO)
I2S4_IN		GPIO18	SD_D1 (IO)			ANTSEL[26] (O)		DBG_UTIF[12] (IO)
I2S2_OUT		GPIO19	SD_D0 (IO)			ANTSEL[27] (O)		DBG_UTIF[13] (IO)
I2S3_OUT		GPIO20	SD_CLK (O)			ANTSEL[28] (O)		DBG_UTIF[14] (IO)
I2S4_OUT		GPIO21	SD_CMD (IO)			ANTSEL[29] (O)		DBG_UTIF[15] (IO)
GPIO_B	GPIO (IO)	GPIO22				ANTSEL[17] (O)		DBG_UTIF[16] (IO)
MDC	MDC (O)	GPIO23						
MDIO	MDIO (IO)	GPIO24						
G2_TXD0	G2_TXD[0] (IO)	GPIO25	SD_D3 (IO)					
G2_TXD1	G2_TXD[1] (IO)	GPIO26	SD_D2 (IO)					
G2_TXD2	G2_TXD[2] (IO)	GPIO27	SD_D1 (IO)					
G2_TXD3	G2_TXD[3] (IO)	GPIO28	SD_D0 (IO)					
G2_TXEN	G2_TXEN (IO)	GPIO29	SD_CLK (O)					
G2_TXC	G2_TXC (IO)	GPIO30	SD_CMD (IO)					
G2_RXD0	G2_RXD[0] (IO)	GPIO31	GPIO (IO)					
G2_RXD1	G2_RXD[1] (IO)	GPIO32	GPIO (IO)					
G2_RXD2	G2_RXD[2] (IO)	GPIO33	GPIO (IO)					
G2_RXD3	G2_RXD[3] (IO)	GPIO34	GPIO (IO)					

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G2_RXDV	G2_RXDV (IO)	GPIO35	GPIO (IO)					
G2_RXC	G2_RXC (IO)	GPIO36	GPIO (IO)					
NCEB	ND_CS_N (O)	GPIO37	GPIO (IO)					DBG_UTIF[18] (IO)
NWEB	ND_WE_N (O)	GPIO38	GPIO (IO)					DBG_UTIF[19] (IO)
NREB	ND_RE_N (O)	GPIO39	GPIO (IO)					DBG_UTIF[20] (IO)
NDL4	ND_D[4] (IO)	GPIO40	EMMC_DATA[4] (IO)					DBG_UTIF[21] (IO)
NDL5	ND_D[5] (IO)	GPIO41	EMMC_DATA[5] (IO)					DBG_UTIF[22] (IO)
NDL6	ND_D[6] (IO)	GPIO42	EMMC_DATA[6] (IO)					DBG_UTIF[23] (IO)
NDL7	ND_D[7] (IO)	GPIO43	EMMC_DATA[7] (IO)					DBG_UTIF[24] (IO)
NRB	ND_RB_N (I)	GPIO44	EMMC_CMD (IO)					DBG_UTIF[25] (IO)
NCLE	ND_CLE (O)	GPIO45	EMMC_CK (O)					DBG_UTIF[26] (IO)
NALE	ND_ALE (O)	GPIO46	GPIO (IO)					DBG_UTIF[27] (IO)
NDL0	ND_D[0] (IO)	GPIO47	EMMC_DATA[0] (IO)					DBG_UTIF[28] (IO)
NDL1	ND_D[1] (IO)	GPIO48	EMMC_DATA[1] (IO)					DBG_UTIF[29] (IO)
NDL2	ND_D[2] (IO)	GPIO49	EMMC_DATA[2] (IO)					DBG_UTIF[30] (IO)
NDL3	ND_D[3] (IO)	GPIO50	EMMC_DATA[3] (IO)					DBG_UTIF[31] (IO)
PMIC_SCL	PMIC_SCL (O)	GPIO71						
PMIC_SDA	PMIC_SDA (IO)	GPIO72						
SPIC1_CLK	SPIC1_CLK (O)	GPIO73	TXD1 (O)	I2C1_SCL (IO)	PWM_CH1 (O)	ANTSEL[12] (O)		DBG_UTIF[0] (IO)
SPIC1_MOSI	SPIC1_MOSI (O)	GPIO74	RXD1 (I)	I2C1_SDA (IO)	PWM_CH2 (O)	ANTSEL[13] (O)		DBG_UTIF[1] (IO)
SPIC1_MISO	SPIC1_MISO (I)	GPIO75	RTS1_N (O)	I2C2_SCL (IO)	PWM_CH3 (O)	ANTSEL[14] (O)		DBG_UTIF[2] (IO)
SPIC1_CS	SPIC1_CS (O)	GPIO76	CTS1_N (I)	I2C2_SDA (IO)	PWM_CH4 (O)	ANTSEL[15] (O)		DBG_UTIF[3] (IO)
GPIO_D	GPIO (IO)	GPIO77			PWM_CH5 (O)	ANTSEL[16] (O)		DBG_UTIF[4] (IO)
WATCHDOG	WATCHDOG (O)	GPIO78			PWM_CH6 (O)			DBG_UTIF[5] (IO)
RTS3_N	RTS3_N (O)	GPIO79		SPIC0_MISO (I)	PCIE0_PAD_WAKE_N (IO)	ANTSEL[18] (O)		DBG_UTIF[6] (IO)
CTS3_N	CTS3_N (I)	GPIO80		SPIC0_CS (O)	PCIE0_PAD_CLKREQ_N (IO)	ANTSEL[19] (O)		DBG_UTIF[7] (IO)
TXD3	TXD3 (O)	GPIO81		SPIC0_CLK (O)	PWM_CH6 (O)	ANTSEL[20] (O)		DBG_UTIF[8] (IO)
RXD3	RXD3 (I)	GPIO82		SPIC0_MOSI (O)		ANTSEL[21] (O)		DBG_UTIF[9] (IO)
PERST0_N	PCIE0_PAD_PERST_N (O)	GPIO83						
PERST1_N	PCIE1_PAD_PERST_N (O)	GPIO84						

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WLED_N	WLED_N (IO)	GPIO85						
EPHY_LED0_N	EPHY_LED0_N (O)	GPIO86						JTRST_N (I)
AUXIN0		GPIO87						
AUXIN1		GPIO88						
AUXIN2		GPIO89						
AUXIN3		GPIO90						
TXD4	TXD4 (O)	GPIO91	EPHY_LED1_N (O)			ANTSEL[0] (O)		JTDI (I)
RXD4	RXD4 (I)	GPIO92	EPHY_LED2_N (O)			ANTSEL[1] (O)		JTDO (O)
RTS4_N	RTS4_N (O)	GPIO93	EPHY_LED3_N (O)			ANTSEL[2] (O)		JTCLK (I)
CTS4_N	CTS4_N (I)	GPIO94	EPHY_LED4_N (O)			ANTSEL[3] (O)		JTMS (IO)
PWM1	PWM_CH1 (O)	GPIO95	RTS4_N (O)	TXD2 (O)		ANTSEL[4] (O)		W_DBGIN (I)
PWM2	PWM_CH2 (O)	GPIO96	CTS4_N (I)	RXD2 (I)		ANTSEL[5] (O)		W_DBGACK (O)
PWM3	PWM_CH3 (O)	GPIO97	TXD4 (O)		AICE_TCKC (I)	ANTSEL[6] (O)		W_JTCLK (I)
PWM4	PWM_CH4 (O)	GPIO98	RXD4 (I)			ANTSEL[7] (O)		W_JTDI (I)
PWM5	PWM_CH5 (O)	GPIO99			AICE_TMSC (IO)	ANTSEL[8] (O)		W_JTMS (I)
PWM6	PWM_CH6 (O)	GPIO100				ANTSEL[9] (O)		W_JTRST_N (I)
PWM7	GPIO (IO)	GPIO101				ANTSEL[10] (O)		DBG_UART_TXD (O)
GPIO_E	GPIO (IO)	GPIO102				ANTSEL[11] (O)		W_JTDO (O)

Note:

"O" = output function

"I" = input function

"IO" = bi-direction function, high active

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2.3.2 xMII PHY/MAC Pin Mapping

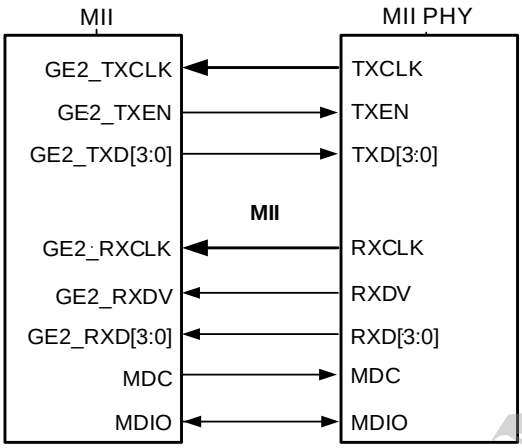

Figure 2-1 MII → MII PHY

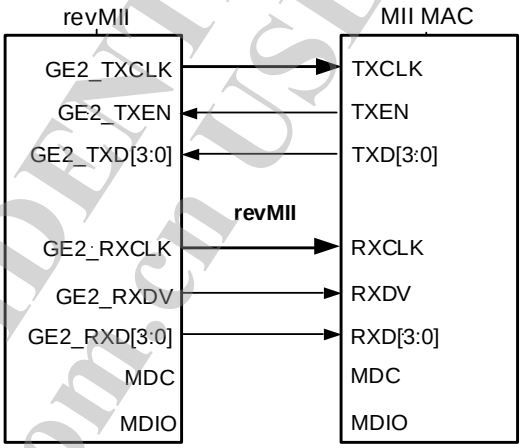

Figure 2-2 revMII → MII MAC

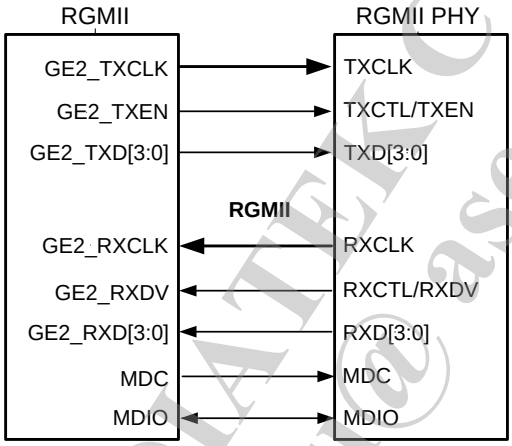

Figure 2-3 RGMII → RGMII PHY

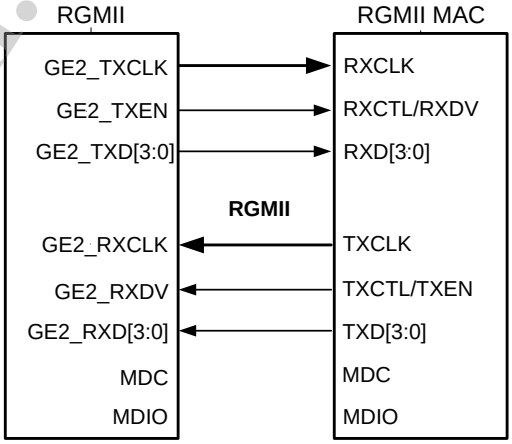

Figure 2-4 RGMII → RGMII MAC

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2.4 Strapping Options

Table 2-6 Strapping

Pin Name	Strapping Name	Description
Bit[1]:NCLE Bit[0]:PMIC_SCL	OSC Selection	0: 25MHz DIP XTAL 1: 25MHz SMD XTAL 2, 3: Reserved
Bit[1]:NREB Bit[0]:NWEB	Boot Order	0: SPI-NOR → eMMC -> SDXC 1: SPI-NAND→ eMMC -> SDXC 2: SLC-NAND → eMMC -> SDXC 3: SDXC→ eMMC -> SLC-NAND
JTAG_MODE	JTAG Mode	0: Normal 1: JTAG mode

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3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol or Pin name	Description	Min.	Max.	Unit
DVDD28_IO1 DVDD28_IO2 DVDD28_IO3	3.3V supply voltage	-0.3	3.6	V
DVDD18_IO1 DVDD18_IO2 DVDD18_IO3 DVDD18_IO4	1.8V supply voltage	-0.3	1.9	V
AVDD33_WF0_PA AVDD33_WF1_PA AVDD33_WF2_PA AVDD33_WF3_PA AVDD33_BT	3.3V supply voltage	-0.3	3.63	V
AVDD33_PMU AVDD33_USB AVDD33_TX AVDD33_TXP0	3.3V supply voltage	-0.3	3.63	V
AVDD22_XO AVDD22_BT AVDD22_WF0_BBPLL AVDD22_WF0 AVDD22_WF3	2.2V supply voltage	-0.3	2.31	V
AVDD18_AP AVDD18_MEMPLL AVDD18_PCIE AVDD18_PLLGP AVDD18_SGMII_SSUSB AVDD18_USB AVDD18_EPHY AVDD18_RTC	1.8V supply voltage	-0.3	1.89	V
DDRVCCIO DDRVCCIO_CLK	1.8V supply voltage	-0.3	1.9	V
	1.5V supply voltage	-0.3	1.9	V
	1.35V supply voltage	-0.3	1.9	V
AVDD10_PCIE0 AVDD10_PCIE1 AVDD10_SGMII AVDD10_SSUSB	1.15V supply voltage	-0.3	1.2	V
AVDD13_WF0_SX AVDD13_WF0_AFE AVDD13_WF3_AFE AVDD13_WF0_TRX	1.45V supply voltage	-0.3	1.52	V

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Symbol or Pin name	Description	Min.	Max.	Unit
AVDD13_WF1_TRX AVDD13_WF2_TRX AVDD13_WF3_TRX AVDD13_BT				
VPROC	1.15V supply voltage	-0.3	1.36	V
VPROC_SRAM	1.15V supply voltage	-0.3	1.36	V
VCCK VCCK_SRAM	1.15V supply voltage	-0.3	1.26	V

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3.2 Recommended Operating Range

Table 3-2 Recommended Operating Range

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD28_IO1 DVDD28_IO2 DVDD28_IO3	3.3V supply voltage	2.97	3.3	3.6	V
DVDD18_IO1 DVDD18_IO2 DVDD18_IO3 DVDD18_IO4	1.8V supply voltage	1.7	1.8	1.9	V
AVDD33_WF0_PA AVDD33_WF1_PA AVDD33_WF2_PA AVDD33_WF3_PA AVDD33_BT	3.3V supply voltage	2.97	3.3	3.63	V
AVDD33_PMU AVDD33_USB AVDD33_TX AVDD33_TXP0	3.3V supply voltage	2.97	3.3	3.63	V
AVDD22_XO AVDD22_BT AVDD22_WF0_BBPLL AVDD22_WF0 AVDD22_WF3	2.2V supply voltage	2.09	2.2	2.31	V
AVDD18_AP AVDD18_MEMPLL AVDD18_PCIE AVDD18_PLLGP AVDD18_SGMII_SSUSB AVDD18_USB AVDD18_EPHY AVDD18_RTC	1.8V supply voltage	1.71	1.8	1.89	V
DDRVCCIO DDRVCCIO_CLK	1.8V supply voltage	1.71	1.8	1.89	V
	1.5V supply voltage	1.425	1.5	1.575	V
	1.35V supply voltage	1.215	1.35	1.485	V
AVDD10_PCIE0 AVDD10_PCIE1 AVDD10_SGMII AVDD10_SSUSB	1.15V supply voltage	1.0925	1.15	1.2075	V
AVDD13_WF0_SX AVDD13_WF0_AFE AVDD13_WF3_AFE AVDD13_WF0_TRX AVDD13_WF1_TRX AVDD13_WF2_TRX AVDD13_WF3_TRX	1.45V supply voltage	1.38	1.45	1.52	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD13_BT	1.45V supply voltage	-	1.45	1.52	V
VPROC	1.15V supply voltage	0.9		1.36	V
VPROC_SRAM	1.15V supply voltage	1.15		1.36	V
VCCK VCCK_SRAM	1.15V supply voltage	1.0925	1.15	1.2075	V

3.3 Thermal Characteristics

Thermal characteristics when stationary without an external heat sink in an air-conditioned environment.

Table 3-3 Thermal Characteristics

Symbol	Description	Performance	
		Typ	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
θ_{JA}	Junction to ambient temperature thermal resistance[1] for JEDEC 2L PCB	24.48	°C/W
θ_{JA}	Junction to ambient temperature thermal resistance[1] for JEDEC 4L PCB	20.09	°C/W
θ_{JC}	Junction to case temperature thermal resistance	2.92	°C/W
θ_{JB}	Junction to case board thermal resistance	10.33	°C/W
Ψ_{Jt}	Junction to the package thermal resistance for JEDEC 2L PCB	1.44	°C/W
Ψ_{Jt}	Junction to the package thermal resistance for JEDEC 4L PCB	1.24	°C/W

Note: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4”x4.5”)

3.4 Operation Conditions

Table 3-4 Operating Conditions

I/O supply voltage	3.3 V +/- 10%
DDR2 supply voltage	1.8 V +/- 5%
DDR3 supply voltage	1.5 V +/- 5% 1.35V+/-5%
Core supply voltage	1.15 V +/- 5%
Ambient Temperature Range	-10 to 70 °C

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3.5 Storage Conditions

The calculated shelf life in a sealed bag is 12 months if stored between 5 °C and 40 °C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168 hours of factory conditions, i.e. < 30 °C at 60% RH.
- Storage humidity needs to maintained at < 10% RH.
- Baking is necessary if the customer exposes the component to air for over 168 hrs, baking conditions: 125 °C for 8 hrs.

3.6 External XTAL Specification

Table 3-5 External XTAL Specifications (RF)

Parameter	Min	Typ	Max	Unit
Frequency		25		MHz
Drive Level			210	uW
Frequency Tolerance	-7		+7	ppm
Series Resistance			30	kΩ
Load Capacitance		16		pF
Shunt Capacitance			7	pF

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3.7 DC Electrical Characteristics

3.7.1 GPIO pins

Table 3-6 GPIO Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_{PU}	Input pull-up resistance	40	75	190	KΩ
R_{PD}	Input pull-down resistance	40	75	190	KΩ
3.3V GPIO					
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	3.9	V
V_{OL}	Output low voltage	-0.3	-	0.4	V
V_{OH}	Output high voltage	2.6	-	3.9	V
1.8V GPIO					
V_{IL}	Input low voltage	-0.3	-	0.6	V
V_{IH}	Input high voltage	1.2	-	2.2	V
V_{OL}	Output low voltage	-0.3	-	0.2	V
V_{OH}	Output high voltage	1.5	-	2.2	V

3.7.1 RGMII pins

Table 3-7 RGMII Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_{PU}	Input pull-up resistance	40	75	190	KΩ
R_{PD}	Input pull-down resistance	40	75	190	KΩ
3.3V RGMII					
V_{IL}	Input low voltage	-0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	3.9	V
V_{OL}	Output low voltage	-0.3	-	0.4	V
V_{OH}	Output high voltage	2.4	-	3.9	V
2.5V RGMII					
V_{IL}	Input low voltage	-0.3	-	0.7	V
V_{IH}	Input high voltage	1.7	-	3.0	V

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V_{OL}	Output low voltage	-0.3	-	0.4	V
V_{OH}	Output high voltage	2.0	-	3.0	V

3.8 AC Electrical Characteristics

3.8.1 SDRAM Interface

3.8.1.1 DDR2

The DDR2 SDRAM interface complies with 533 MHz timing requirements for standard DDR2 SDRAM. The interface drivers are SSTL_18 drivers matching the EIA/JEDEC standard JESD208.

Table 3-8 DDR2 SDRAM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Average clock period	1875	7500	ps	
tCH(avg)	Average clock high pulse width	0.48	0.52	tCK(avg)	
tCL(avg)	Average clock low pulse width	0.48	0.52	tCK(avg)	
tCH(abs)	Absolute clock high pulse width	0.44	0.53	tCK(avg)	
tCL(abs)	Absolute clock low pulse width	0.44	0.53	tCK(avg)	
tCKE	CKE min. pulse width	3	-	tCK(avg)	
tIS(base)	Address and control input setup time	125	-	ps	
tIH(base)	Address and control input setup time	200	-	ps	
tIS	Command/Address setup time to CK	tIS(base)+ △tIS	-	ps	
tIH	Command/Address hold time from CK	tIH(base)+ △tIH	-	ps	
tDQSCK	DQS output access time from SDRAM CLK	-325	325	ps	
tDQSQ	Data skew of DQS and associated DQ	-	175	ps	
tQHS	Data hold skew factor	-	250	ps	
tQH	DQ/DQS output hold time from DQS	tHP - tQHS	-	ns	
tRPRE	Read preamble	0.9	1.1	tCK(avg)	
tRPST	Read postamble	0.4	0.6	tCK(avg)	
tDH(base)	DQ and DM input hold time	75	-	ps	
tDS(base)	DQ and DM input hold time	0	-	ps	

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Symbol	Description	Min	Max	Unit	Remark
tDH	DQ and DQM input hold time	tDH(base)+△tDH	-	ps	
tDS	DQ and DQM input setup time	tDS(base)+△tDS	-	ps	
tDIPW	DQ and DM input pulse width	0.35	-	tCK(avg)	
tDQSS	Write command to 1st DQS latching transition	-0.25	0.25	tCK(avg)	
tDQSH	DQS input high pulse width	0.35	-	tCK(avg)	
tDQSL	DQS input low pulse width	0.35	-	tCK(avg)	
tDSS	DQS falling edge setup time to CK	0.2	-	tCK(avg)	
tDSH	DQS falling edge hold time from CK	0.2	-	tCK(avg)	
tWPRE	DQS write preamble	0.35	-	tCK(avg)	
tWPST	DQS write postamble	0.4	-	tCK(avg)	

3.8.1.2 DDR3

The DDR3 SDRAM interface complies with 800 MHz timing requirements for standard DDR3 SDRAM. The interface drivers are SSTL_15 drivers matching the EIA/JEDEC standard JESD79-3E.

Table 3-9 DDR3 SDRAM Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCK(avg)	Average clock period	1.25	-	ns	
tCH(avg)	Average clock high pulse width	0.47	0.53	tCK(avg)	
tCL(avg)	Average clock low pulse width	0.47	0.53	tCK(avg)	
tCH(abs)	Absolute clock high pulse width	0.43	-	tCK(avg)	
tCL(abs)	Absolute clock low pulse width	0.43	-	tCK(avg)	
tIS	Command/Address setup time to CK	170	-	ps	
tIH	Command/Address hold time from CK	120	-	ps	
tDQSCK	DQS output access time from CK	-225	225	ps	
tDQSQ	Data skew of DQS and associated DQ	-	100	ps	
tQSH	DQS output high time	0.4	-	tCK(avg)	
tQSL	DQS output low time	0.4	-	tCK(avg)	
tQH	DQ/DQS output hold time from DQS	0.38	-	tCK(avg)	
tRPRE	DQS read preamble	0.9	-	tCK(avg)	
tRPST	DQS read postamble	0.3	-	tCK(avg)	
tDH	DQ hold time from DQS	45	-	ps	

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Symbol	Description	Min	Max	Unit	Remark
tDS	DQ setup time to DQS	10	-	ps	
tDIPW	DQ and DM input pulse width	360	-	Ps	
tDQSS	DQS rising edge to CK rising edge	-0.27	0.27	tCK(avg)	
tDQSH	DQS input high pulse width	0.45	0.55	tCK(avg)	
tDQSL	DQS input low pulse width	0.45	0.55	tCK(avg)	
tDSS	DQS falling edge setup time to CK	0.18	-	tCK(avg)	
tDSH	DQS falling edge hold time from CK	0.18	-	tCK(avg)	
tWPRE	DQS write preamble	0.9	-	tCK(avg)	
tWPST	DQS write postamble	0.3	-	tCK(avg)	

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3.8.2 RGMII Interface

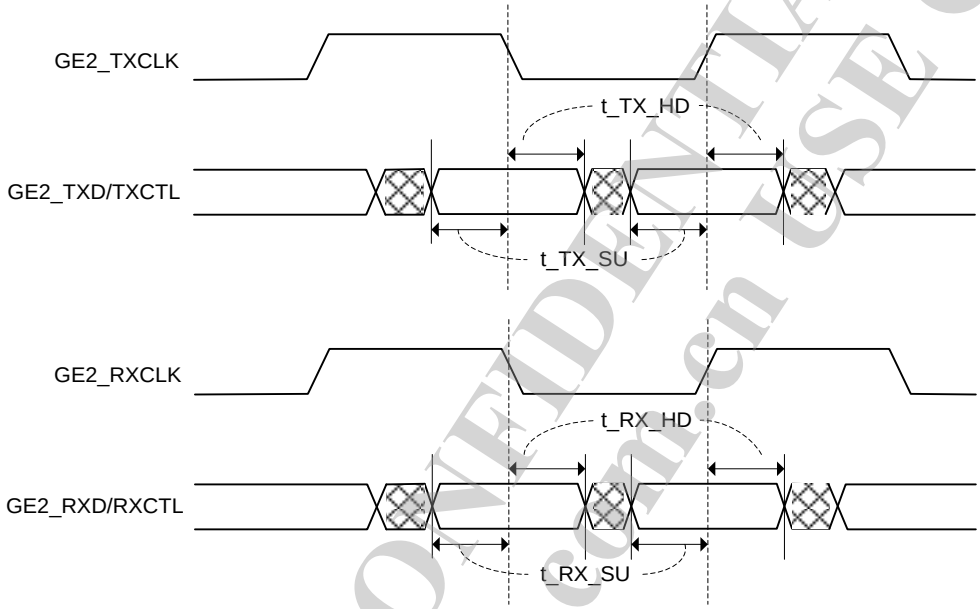

Figure 3-1 RGMII Timing

Table 3-10 RGMII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_SU	Setup time for output signals (e.g. GE0_TXD*, GE0_TXEN)	1.2	-	ns	output load: 5 pF
t_TX_HD	Hold time for output signals	1.2	-	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	1.0	-	ns	
t_RX_HD	Hold time for input signals	1.0	-	ns	

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3.8.3 MII Interface (25 MHz)

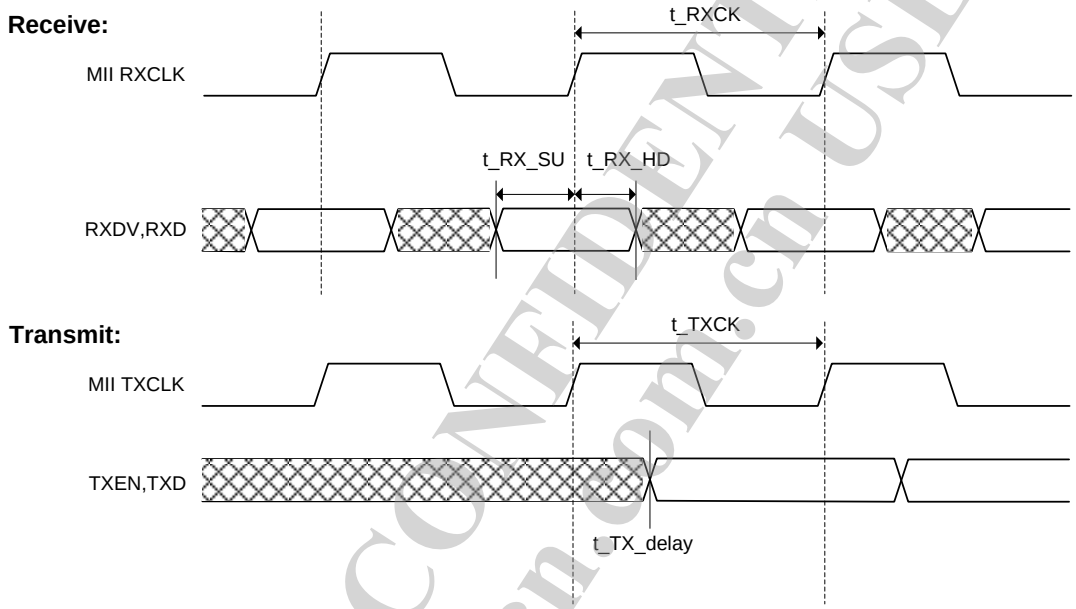

Figure 3-2 MII Timing

Table 3-11 MII Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_delay	Delay to output signals (e.g. GE0_TXD*, GE0_TXEN)	6	22	ns	output load: 5 pF
t_RX_SU	Setup time for input signals (e.g. GE0_RXD*, GE0_RXDV)	10	-	ns	
t_RX_HD	Hold time for input signals	5	-	ns	

Note: For 25 Mhz TXCLK & RXCLK

3.8.4 MDIO Interface

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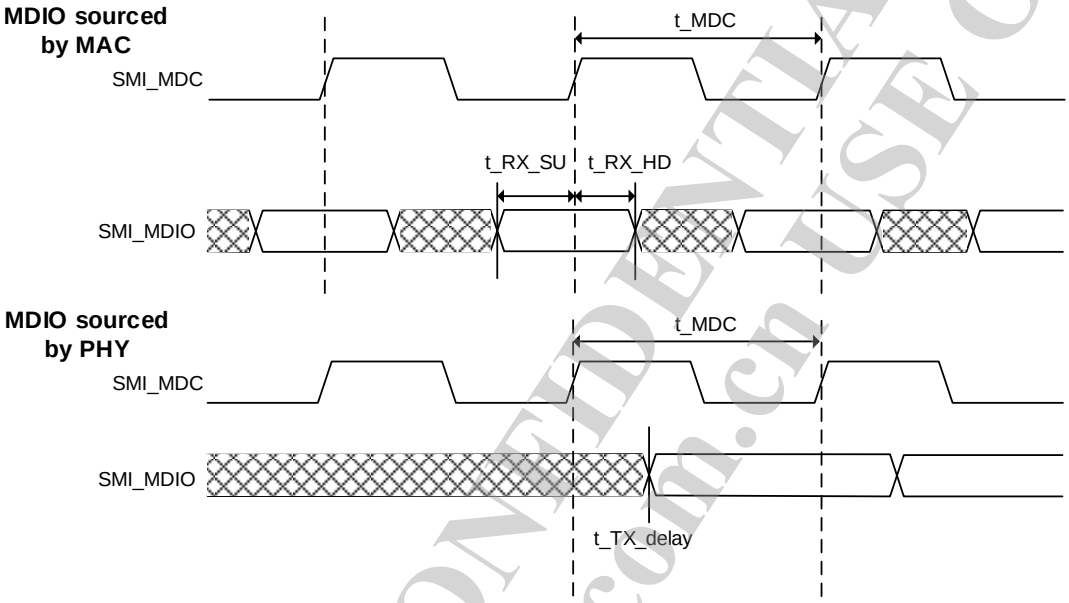

Figure 3-3 SMI MDIO Timing

Table 3-12 SMI Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_TX_delay	Clock to output delay from the PHY	0	300	ns	
t_RX_SU	Setup time referenced to the rising edge of SMI_MDC	10	-	ns	
t_RX_HD	Hold time referenced to the rising edge of SMI_MDC	10	-	ns	

Note: For 2.5 MHz SMI_MDC

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3.8.5 UART Interface

MT7622 utilizes the Universal Asynchronous Receiver Transmitter (UART) interface as its host control interface. The electrical timing characteristic for the UART interface is illustrated below.

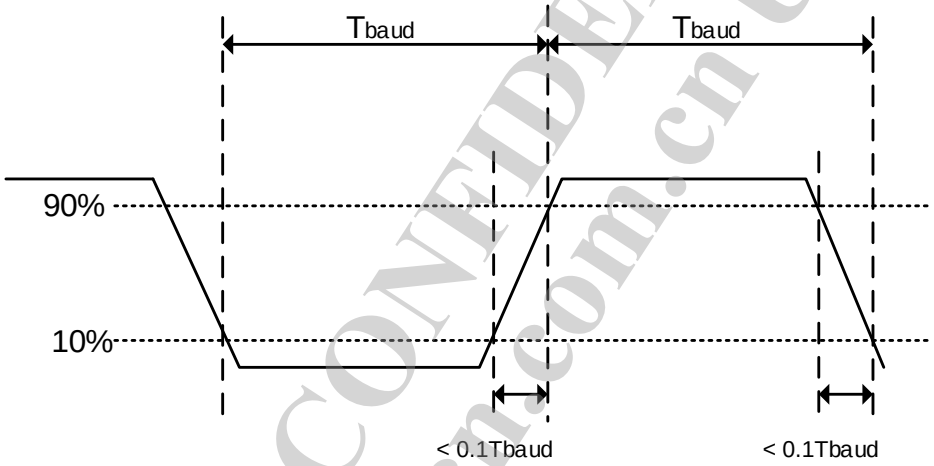

Figure 3-4 UART Timing

3.8.6 eMMC Interface

3.8.6.1 High-Speed (SDR) Mode

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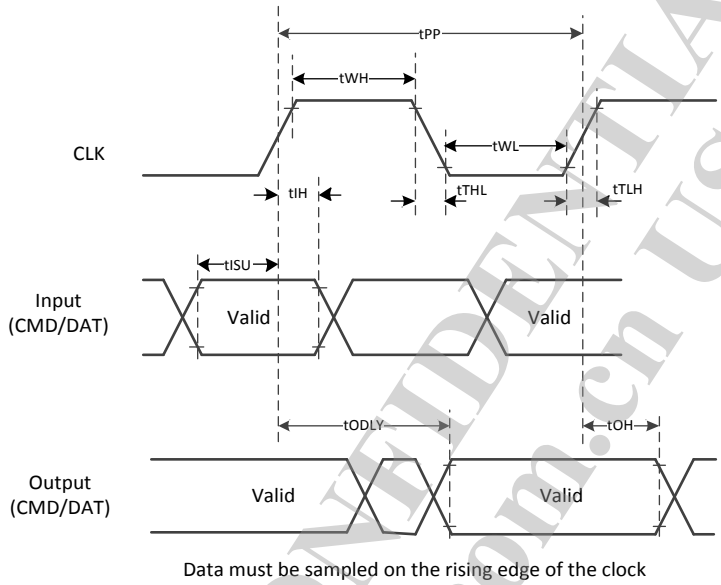

Figure 3-5 Timing Diagram - Data Input/Output

Table 3-13 High-Speed device Interface Timing

Symbol	Description	Min	Max	Unit	Remark
Clock CLK[1]					
fPP	Clock frequency Data Transfer Mode (PP)[2]	0	52[3]	MHz	
tWH	Clock high time	6.5		ns	
tWL	Clock low time	6.5		ns	
tTLH	Clock rise time[4]		3	ns	
tTHL	Clock fall time		3	ns	
Input CMD,DAT(referenced to CLK)					
tISU	Input setup time	3		ns	
tIH	Input hold time	3		ns	
Output CMD,DAT(referenced to CLK)					
tODLY	Output delay time during data transfer		13.7	ns	
tOH	Output hold time	2.5		ns	
tRISE	Signal rise time[5]		3	ns	
tFALL	Signal fall time		3	ns	

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Symbol	Description	Min	Max	Unit	Remark
NOTE 1 CLK timing is measured at 50% of V_{CCQ}. NOTE 2 A *e*•MMC shall support the full frequency range from 0 Mhz - 26 Mhz, or 0 MHz - 52 MHz NOTE 3 Device can operate as high-speed Device interface timing at 26 MHz clock frequency. NOTE 4 CLK rise and fall times are measured by min (V_{IH}) and max (V_{IL}). NOTE 5 Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).					

3.8.6.2 High-Speed (DDR) Mode

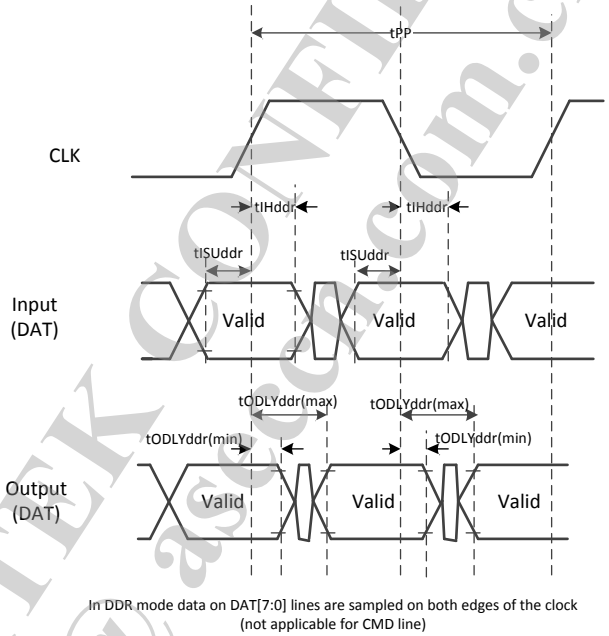

Figure 3-6 Timing Diagram - Data Input/Output in Dual Data Rate Mode

Table 3-14 High-Speed Dural Rate Interface Timing

Symbol	Description	Min	Max	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
tTLH	Clock rise time		3	ns	
tTHL	Clock fall time		3	ns	
Input CMD (referenced to CLK-SDR mode)					
tISUddr	Input setup time	3		ns	

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Symbol	Description	Min	Max	Unit	Remark
tIHddr	Input hold time	3		ns	
Output CMD(referenced to CLK-SDR mode)					
tODLY	Output delay time during data transfer		13.7	ns	
tOH	Output hold time	2.5		ns	
tRISE	Signal rise time		3	ns	
tFALL	Signal fall time		3	ns	
Input DAT (referenced to CLK-DDR mode)					
tISUddr	Input setup time	2.5		ns	
tIHddr	Input hold time	2.5		ns	
Output DAT(referenced to CLK-DDR mode)					
tODLYddr	Output delay time during data transfer	1.5	7	ns	
tRISE	Signal rise time[2]		2	ns	
tFALL	Signal fall time		2	ns	

NOTE 1 CLK timing is measured at 50% of V_{CCQ}.
NOTE 2 Inputs DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL})

3.8.7 SD Interface

3.8.7.1 High-Speed Mode

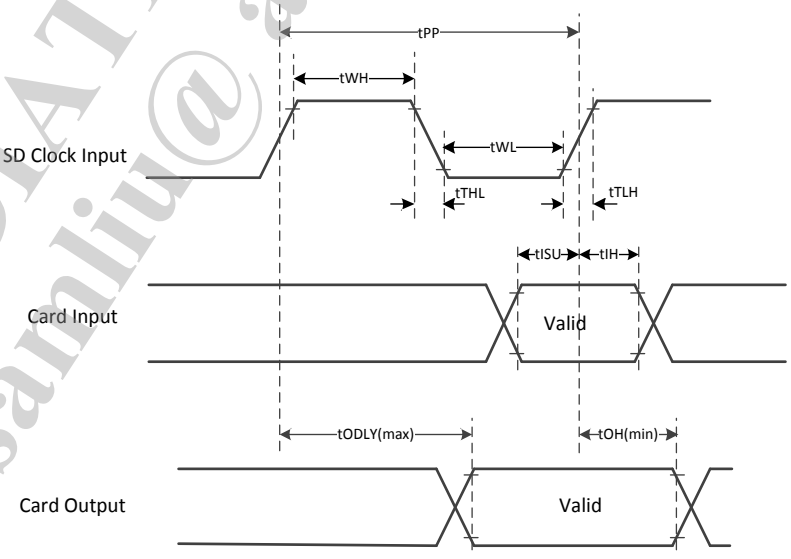

Figure 3-7 Timing Diagram - Card Input/Output Timing(High-Speed Card)

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Table 3-15 Bus Timing Parameter Values (High-Speed)

Symbol	Description	Min	Max	Unit	Remark
Clock CLK[1](All values are referred to min(V_{IH}) and max(V_{IL}))					
fPP	Clock frequency Data Transfer Mode	0	50	MHz	
tWH	Clock high time	7		ns	
tWL	Clock low time	7		ns	
tTLH	Clock rise time[4]		3	ns	
tTHL	Clock fall time		3	ns	
Input CMD,DAT(referenced to CLK)					
tISU	Input setup time	6		ns	
tIH	Input hold time	2		ns	
Output CMD,DAT(referenced to CLK)					
tODLY	Output delay time during data transfer		14	ns	
tOH	Output hold time	2.5		ns	

3.8.8 I2C Interface

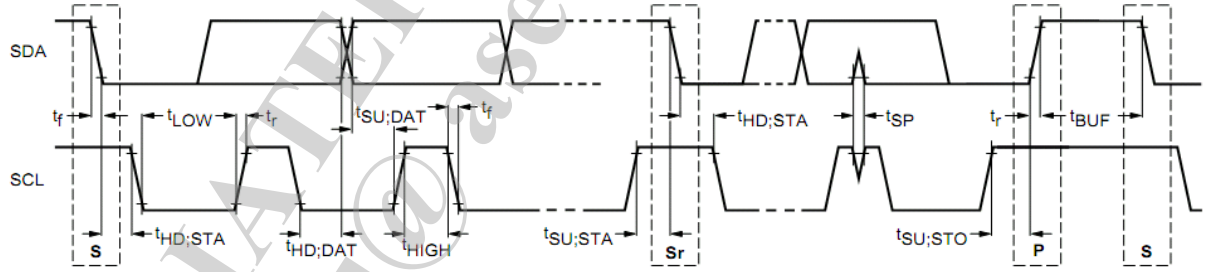

Figure 3-8 I2C Timing

Table 3-16 I2C Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
fSCL	SCL clock frequency	0	400	kHz	
tBUF	Bus free time between a STOP and START condition	1.3	-	us	
tHD	Hold time (repeated) START condition. After this period, the first clock pulse is generated	-	-	us	

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Symbol	Description	Min	Max	Unit	Remark
tLOW	LOW period of the SCL clock	1.3	-	us	
tHIGH	HIGH period of the SCL clock	0.6		us	
tSU:STA	Setup time for a repeated START condition	0.6	-	us	
THD:DAT	Data hold time:	-	-	us	
tSU:DAT	Data setup time	100	-	ns	
tr	Rise time of both SDA and SCL signals	20	300	ns	
tf	Fall time of both SDA and SCL signals	20	300	ns	
tSU:STO	Setup time for STOP condition	0.6	-	us	

3.8.9 SPI Interface

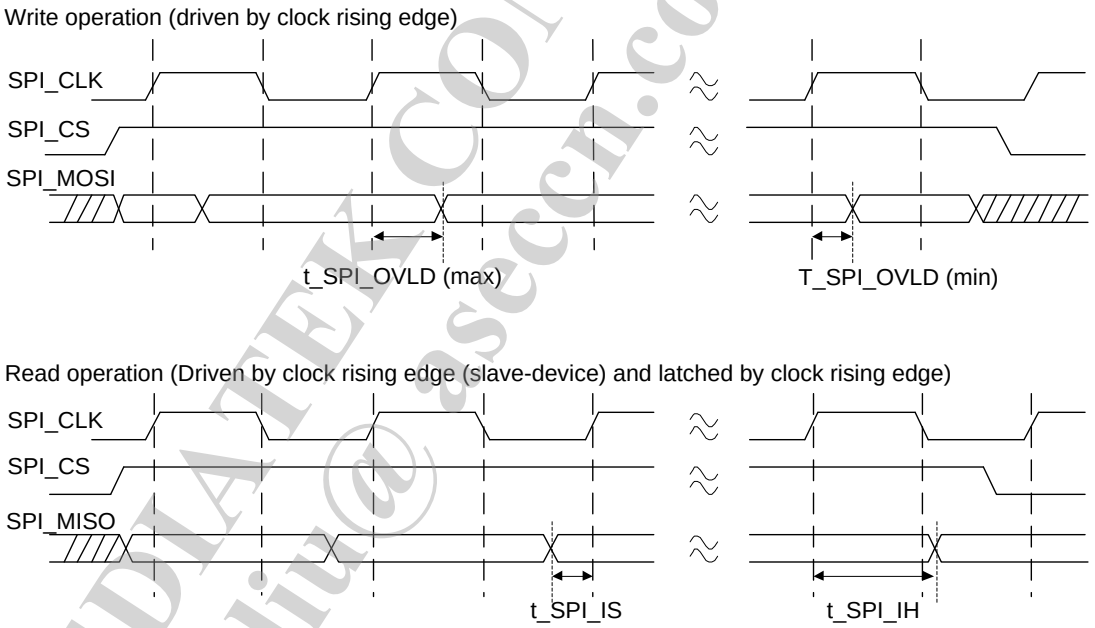

Figure 3-9 SPI Timing

Table 3-17 SPI Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
t_SPI_IS	Setup time for SPI input	6.0	-	ns	
t_SPI_IH	Hold time for SPI input	-1.0	-	ns	
t_SPI_OVLD	SPI_CLK to SPI output valid	-2.0	3.0	ns	output load: 5 pF

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3.8.10 SPI NOR Flash Interface

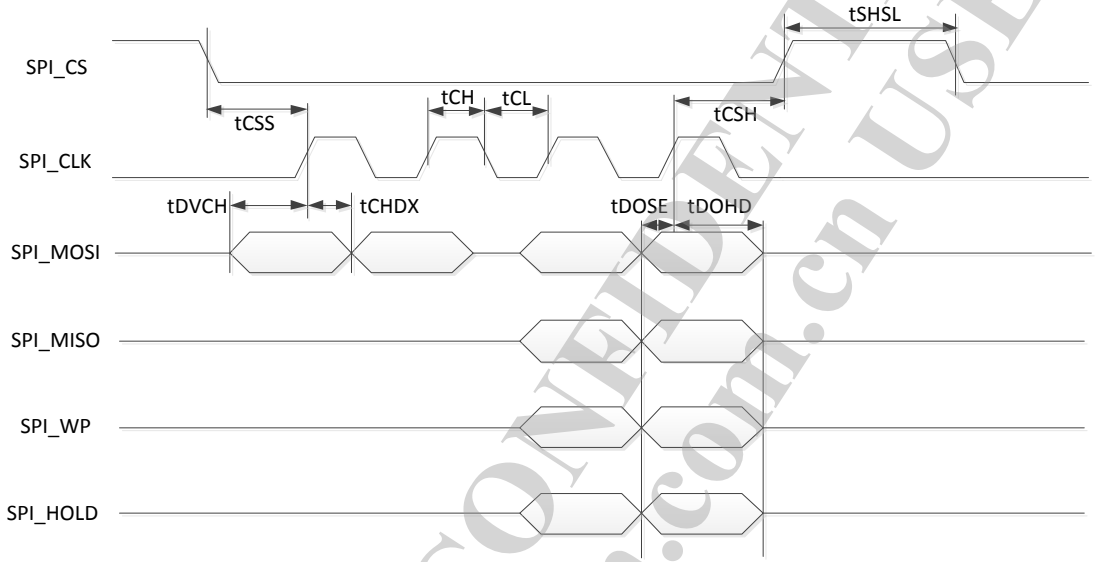

Figure 3-10 SPI NOR interface timing

Table 3-18 SPI NOR Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
fC	Clock frequency	-	50	MHz	
tCH	Clock High Time (relative to CK)	6.1	6.8	ns	
tCL	Clock Low Time (relative to CK)	6.3	6.9	ns	
tSHSL	CS deselect time	88	-	ns	
tCSS	CS active Setup time	42	-	ns	
tCSH	CS active Hold time	67	-	ns	
tDVCH	DI setup time	5.7	-	ns	
tCHDX	DI hold time	6.3	-	ns	
tDOSE	DO setup time	0	-	ns	
tDOHD	DO hold time	3	-	ns	

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3.8.11 NAND Flash Interface

3.8.11.1 Parallel NAND (Samsung Compatible Device)

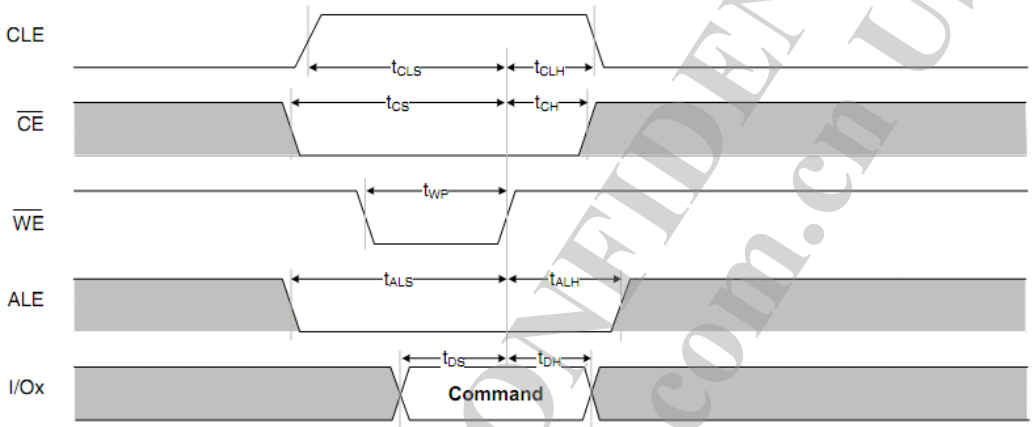

Figure 3-11 Parallel NAND Flash Command Timing

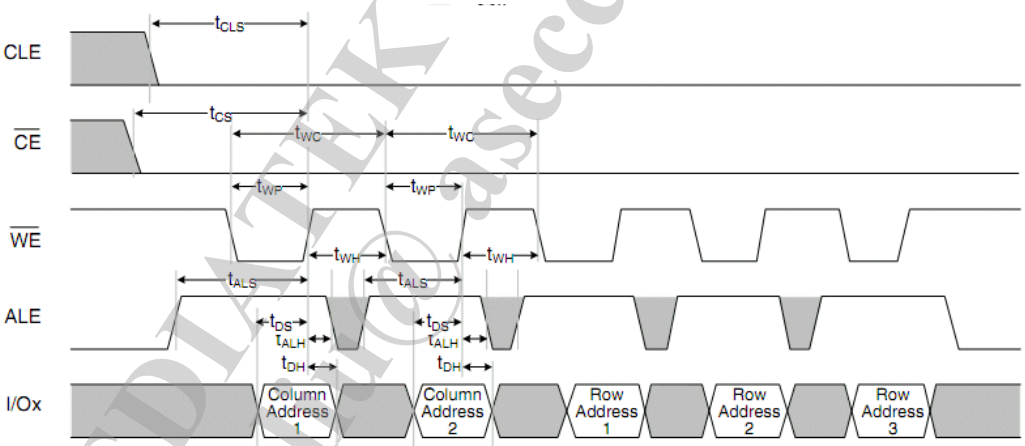

Figure 3-12 Parallel NAND Flash Address Latch Timing

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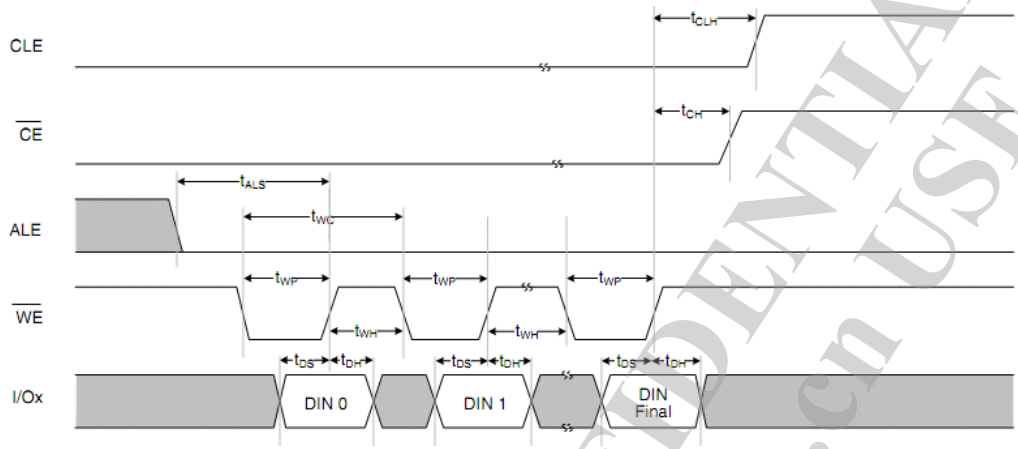

Figure 3-13 Parallel NAND Flash Write Timing

Table 3-19 Parallel NAND Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCLS	CLE setup time	12	-	ns	
tCLH	CLE hold time	5		ns	
tCS	CE setup time	20		ns	
tCH	CE hold time	5		ns	
tWP	WE pulse width	12		ns	
tALS	ALE setup time	12		ns	
tALH	ALE hold time	5		ns	
tDS	Data setup time	12		ns	
tDH	Data hold time	5		ns	
tWC	Write cycle time	25		ns	
tWH	WE high hold time	10		ns	

3.8.11.2 SPI NAND (Winbond Compatible Device)

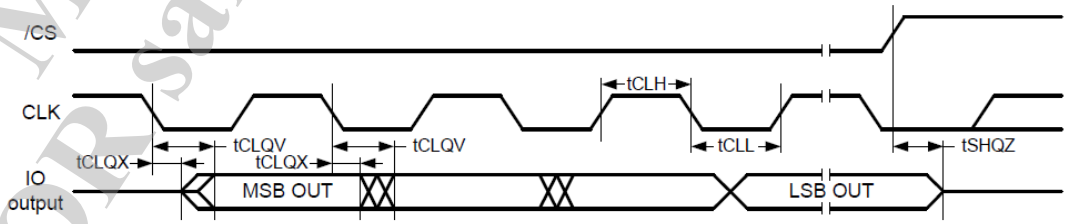

Figure 3-14 SPI NAND Serial Output Timing

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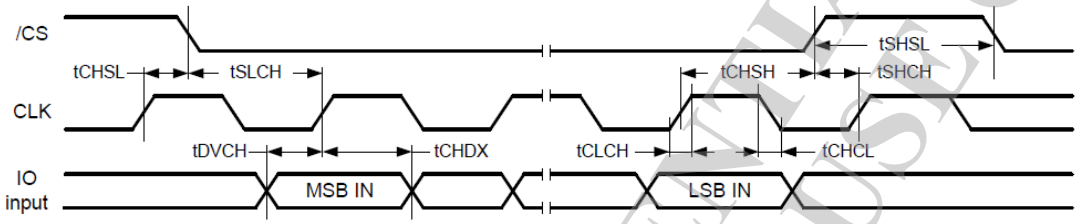

Figure 3-15 SPI NAND Serial Input Timing

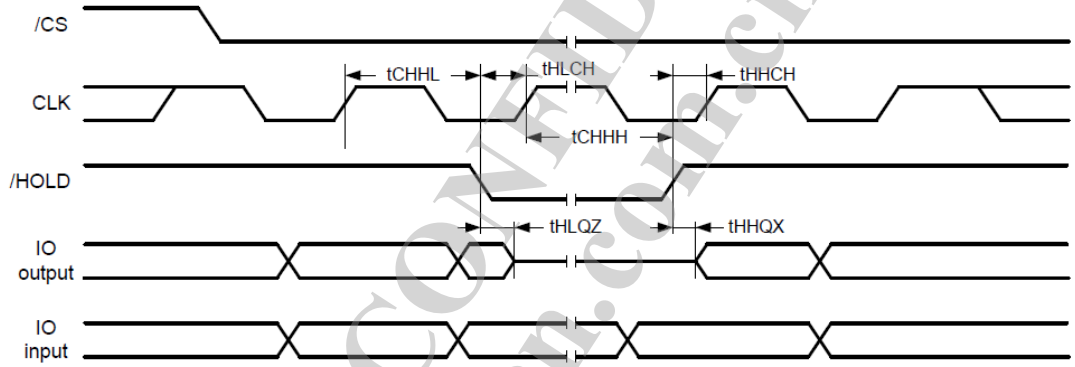

Figure 3-16 SPI NAND /HOLD Timing

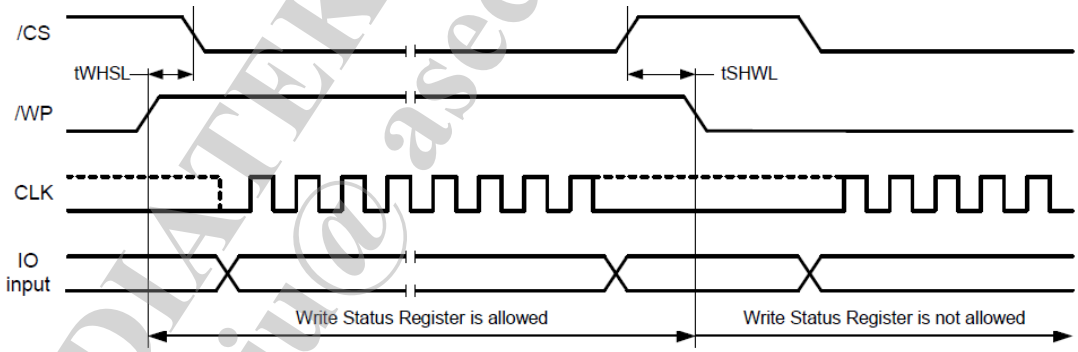

Figure 3-17 SPI NAND /WP Timing

Table 3-20 SPI NAND Interface Diagram Key

Symbol	Description	Min	Max	Unit	Remark
tCLH, tCLL,	Clock High, Low Time for all instructions	4	-	ns	
tCLCH	Clock Rise Time peak to peak	0.1		V/ns	
tCHCL	Clock Fall Time peak to peak	0.1		V/ns	
tSLCH	/CS Active Setup Time relative to CLK	5		ns	

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Symbol	Description	Min	Max	Unit	Remark
tCLCH	/CS Not Active Hold Time relative to CLK	5		ns	
tDVCH	Data in Setup Time	2		ns	
tCHDX	Data in Hold Time	3		ns	
tCHSH	/CS Active Hold Time relative to CLK	3		ns	
tSHCH	/CS Not Active Setup Time relative to CLK	3		ns	
tSHSL1	/CS Deselect Time(for Array Read → Array Read)	10		ns	
tSHSL2	/CS Deselect Time(for Erase, Program or Read Status Registers → Read Status Registers)	50		ns	
tSHQZ	Output Disable Time		7	ns	
tCLQV	Clock Low to Output Valid		7	ns	
tCLQX	Output Hold Time	2		ns	
tHLCH	/HOLD Active Setup Time relative to CLK	5		ns	
tCHHH	/HOLD Active Hold Time relative to CLK	5		ns	
tHHCH	/HOLD Not Active Setup Time relative to CLK	5		ns	
tCHHL	/HOLD Not Active Hold Time relative to CLK	5		ns	
tHHQX	/HOLD to Output Low-Z		7	ns	
tHLQZ	/HOLD to Output High-Z		12	ns	
tWHSL	Write Protect Setup Time Before /CS Low	20		ns	
tSHWL	Write Protect Hold Time After /CS High	100		ns	
tW	Status Register Write Time		50	ns	
tRST	/CS High to next Instruction after Reset during Page Data Read / Program Execute / Block Erase		5/10/500	ns	
tRD1	Read Page Data Time (ECC disabled)		25	us	
tRD2	Read Page Data Time (ECC enabled)		60	us	

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3.9 Power on Sequence

Figure 3-18 Power ON Sequence

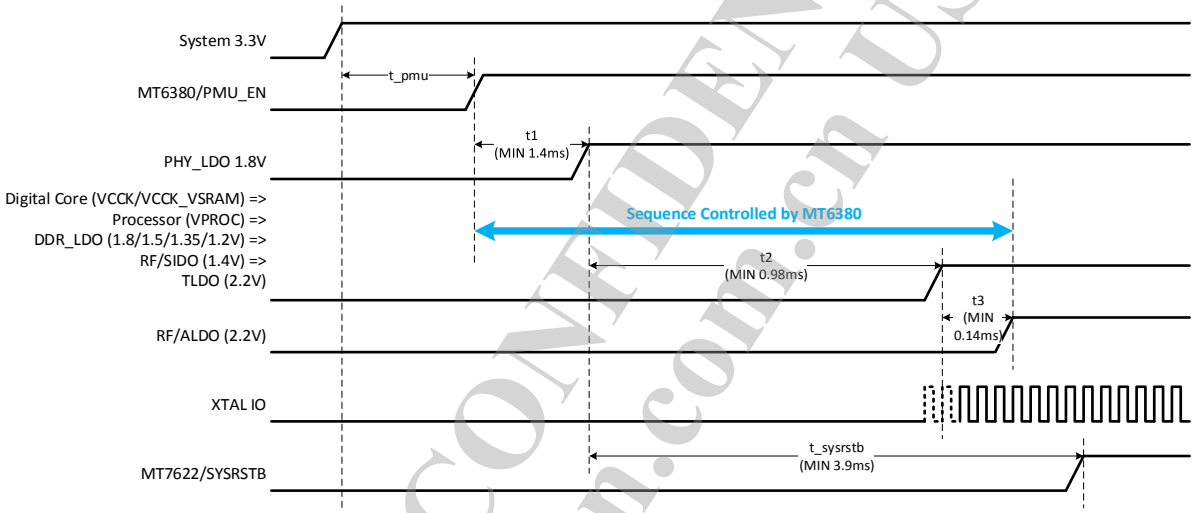

Table 3-21 Power ON Sequence Diagram Key

Symbol	Symbol	Min	Max	Unit
t1	PMU_EN @1.4V (Vth) to PHY_LDO power (1.8V)	1.4	4.3	ms
t2	PHY_LDO power (1.8V) to TLDO XTAL power (2.2V)	0.98	3.00	ms
t3	TLDO XTAL power (2.2V) to RF ALDO power (2.2V)	0.14	0.43	ms
t_pmu	Board 3.3V power to PMU_EN assertion @1.4V (Vth)	0	-	ms
t_sysrstb	PHY_LDO power (1.8V) to PAD_SYSRSTB de-assertion	3.9	-	ms

3.10 WiFi RF Specification

The section describes the WiFi Tx and Rx static performance which is defined at the antenna port, the RF front-end loss is near 0.5dB, and at the normal temperature.

3.10.1 Wi-Fi 2.4GHz Band RF Receiver Specifications

Table 3-22. 2.4GHz RF receiver specifications

Parameter	Description	Performance

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		Min.	Typ.	Max.	Unit
Frequency range		2412	-	2484	MHz
RX sensitivity	1 Mbps DSSS	-	-97.5	-	dBm
	2 Mbps DSSS	-	-94.5	-	dBm
	5.5 Mbps CCK	-	-92.5	-	dBm
	11 Mbps CCK	-	-89.5	-	dBm
RX sensitivity	6 Mbps OFDM	-	-95	-	dBm
	9 Mbps OFDM	-	-92.5	-	dBm
	12 Mbps OFDM	-	-91.5	-	dBm
	18 Mbps OFDM	-	-89	-	dBm
	24 Mbps OFDM	-	-86	-	dBm
	36 Mbps OFDM	-	-82.5	-	dBm
	48 Mbps OFDM	-	-78.5	-	dBm
	54 Mbps OFDM	-	-77	-	dBm
RX sensitivity BW=20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-94	-	dBm
	MCS 1	-	-91	-	dBm
	MCS 2	-	-88.5	-	dBm
	MCS 3	-	-85.5	-	dBm
	MCS 4	-	-82	-	dBm
	MCS 5	-	-77.5	-	dBm
	MCS 6	-	-76	-	dBm
	MCS 7	-	-75	-	dBm
	MCS 31	-	-74	-	dBm
RX sensitivity BW=40MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-91	-	dBm
	MCS 1	-	-88	-	dBm
	MCS 2	-	-85.5	-	dBm
	MCS 3	-	-82	-	dBm
	MCS 4	-	-79	-	dBm
	MCS 5	-	-74.5	-	dBm
	MCS 6	-	-73	-	dBm
	MCS 7	-	-72	-	dBm
	MCS 31	-	-71	-	dBm
Maximum receive level	11 Mbps CCK	-	-5	-	dBm
	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive adjacent channel rejection	1 Mbps DSSS	-	Note*	-	dB
	11 Mbps CCK	-	Note*	-	dB
	6 Mbps OFDM	-	Note*	-	dB
	54 Mbps OFDM	-	Note*	-	dB
Receive adjacent channel rejection (HT20)	MCS 0	-	Note*	-	dB
	MCS 7	-	Note*	-	dB
Receive adjacent	MCS 0	-	Note*	-	dB

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Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
channel rejection (HT40)	MCS 7	-	Note*	-	dB

Note*: Receive adjacent channel rejection comply IEEE spec.

3.10.2 Wi-Fi 2.4GHz Band RF Transmitter Specifications

Table 3-23. 2.4GHz RF transmitter specifications

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2412	-	2484	MHz
Output power	1~11 Mbps CCK/DSSS	-	22	-	dBm
	6 Mbps OFDM	-	20.5	-	dBm
	54 Mbps OFDM	-	19	-	dBm
	HT40, MCS 0	-	19.5	-	dBm
	HT40, MCS 7	-	17.5	-	dBm
Output power variation[1]	TSSI closed-loop control across temperature and channels and VSWR ≦ 1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic output power[2]	2nd Harmonic	-	-48	-	dBm/MHz
	3rd Harmonic	-	-48	-	dBm/MHz

Note 1: VDD33 voltage is within ±5% of typical value.

Note2: Second and third harmonic level measured when shielding cover is added

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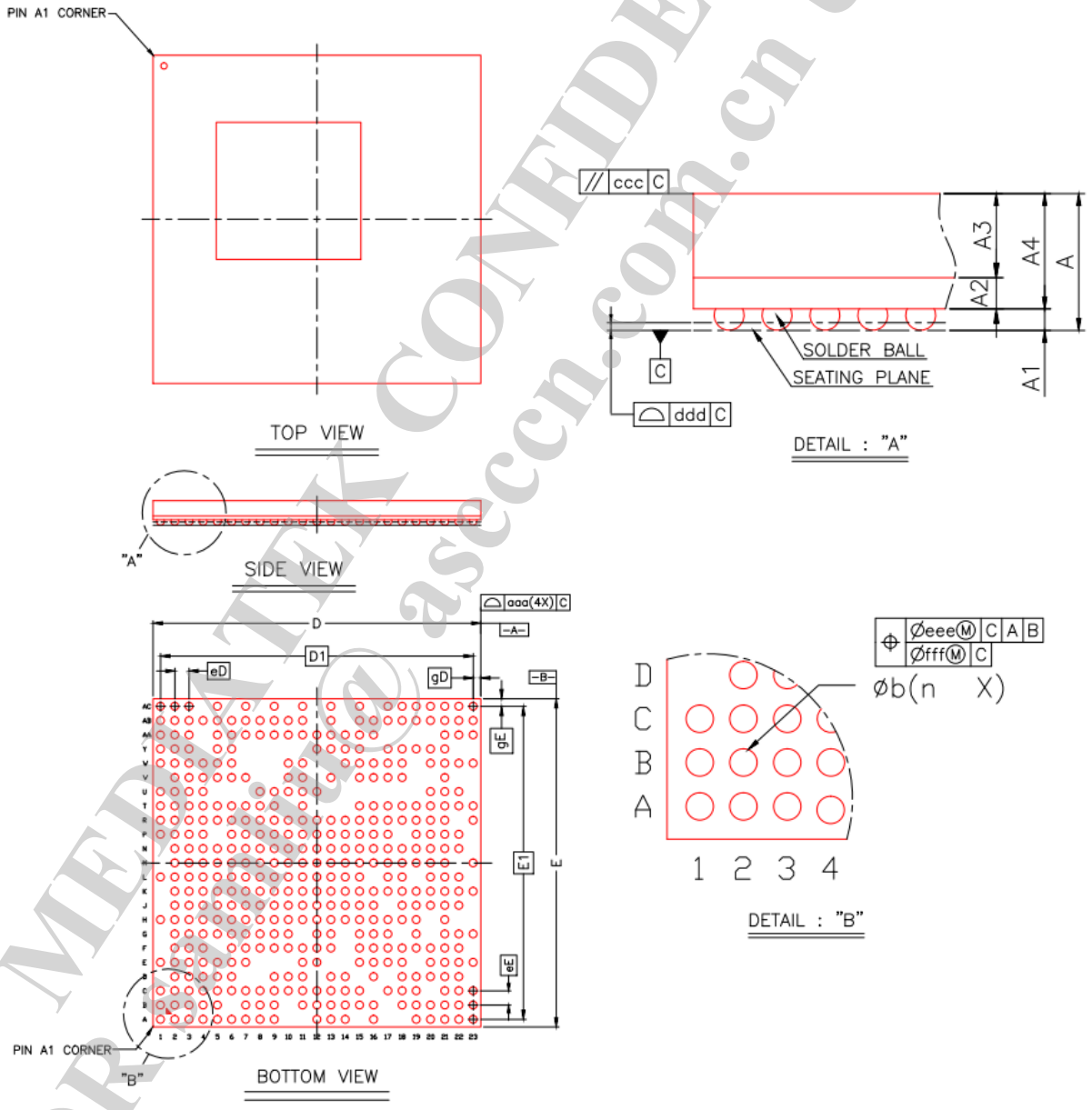
4 Package Information

4.1 Dimensions - FCCSP (15 x 15mm)

Figure 4-1 Package Dimension



NOTE:

1. Controlling dimensions are in millimeters.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.

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3. The pattern of pin 1 fiducial is for reference only.

4.1.1 Diagram Key

Table 4-1 Package Diagram Key

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	14.90	15.00	15.10
	Y	E	14.90	15.00	15.10
Ball Pitch	X	eD		0.65	
	Y	eE		0.65	
Mold Thickness		A3		0.70 Ref.	
Substrate Thickness		A2		0.178 Ref.	
Substrate+Mold Thickness		A4	0.828	0.878	0.928
Total Thickness		A	–	–	1.20
Ball Diameter				0.35	
Ball Stand Off		A1	0.20	0.25	0.30
Ball Width		b	0.30	0.35	0.40
Package Edge Tolerance		aaa		0.10	
Mold Flatness		ccc		0.15	
Coplanarity		ddd		0.10	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		426	
Edge Ball Center to Center	X	D1		14.30	
	Y	E1		14.30	
Edge Ball Center to Package Edge	X	gD		0.35	
	Y	gE		0.35	

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4.2 Reflow Profile Guideline

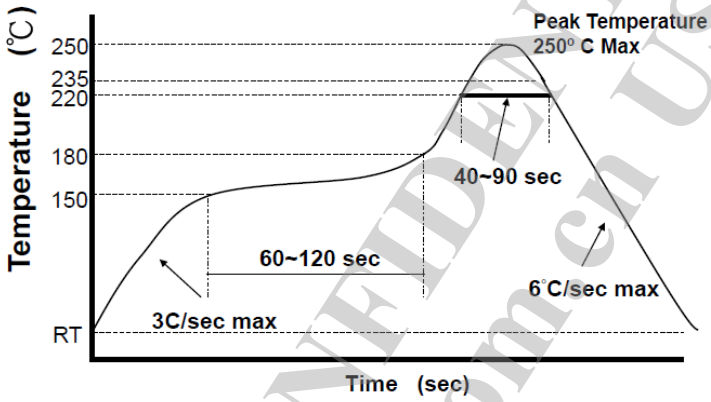

Figure 4-2 Reflow profile

Notes:

1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

.

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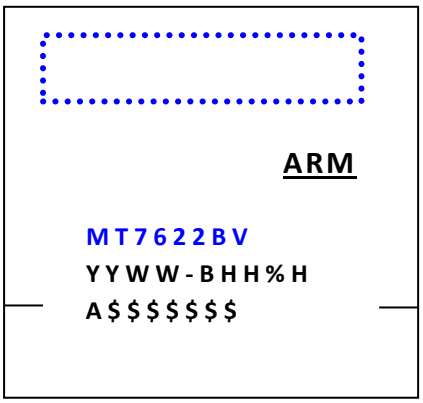
4.3 Top Marking



%: Subcontractor Code

$$$$$$$: LOT NO.

YYWW: date code

: Boundary of EMI conductive Tape

Figure 4-3 MT7622BV/BHHA-H Top marking

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4.4 Ordering Information

Part Number	Package (Green/RoHS Compliant)
MT7622B	15 x 15 mm, 426-balls FCCSP

Note: a heat sink is required in max ambient temperature.

1.

2.

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